ATLAS at LBNL

Physics Division

M.Barnett, A. Ciocio, S, Dardin, K. Einsweiler, V. Fadeyev, M. Garcia-Sciveres, M. Gilchriese, F. Goozen, C. Haber, I. Hinchliffe, S. Loken, F. McCormack, J. Richardson, A. Saavedra, M. Shapiro, J. Siegrist, H. Spieler, J. Taylor, G. Trilling, L. Vacavant, T. Weber, R. Witharm

NERSC

P. Calafiura, C. Day, C. Leggett, M. Marino, D. Quarrie, C. Tull

Engineering Division

E. Anderssen, L. Blanquart, P. Denes, N. Hartman, B. Holmes, T. Johnson, J. Joseph, E. Mandelli, G. Meddeler, V. Risk, C. Tran, C. Vu, J. Wirth, G. Zizka

Visitors

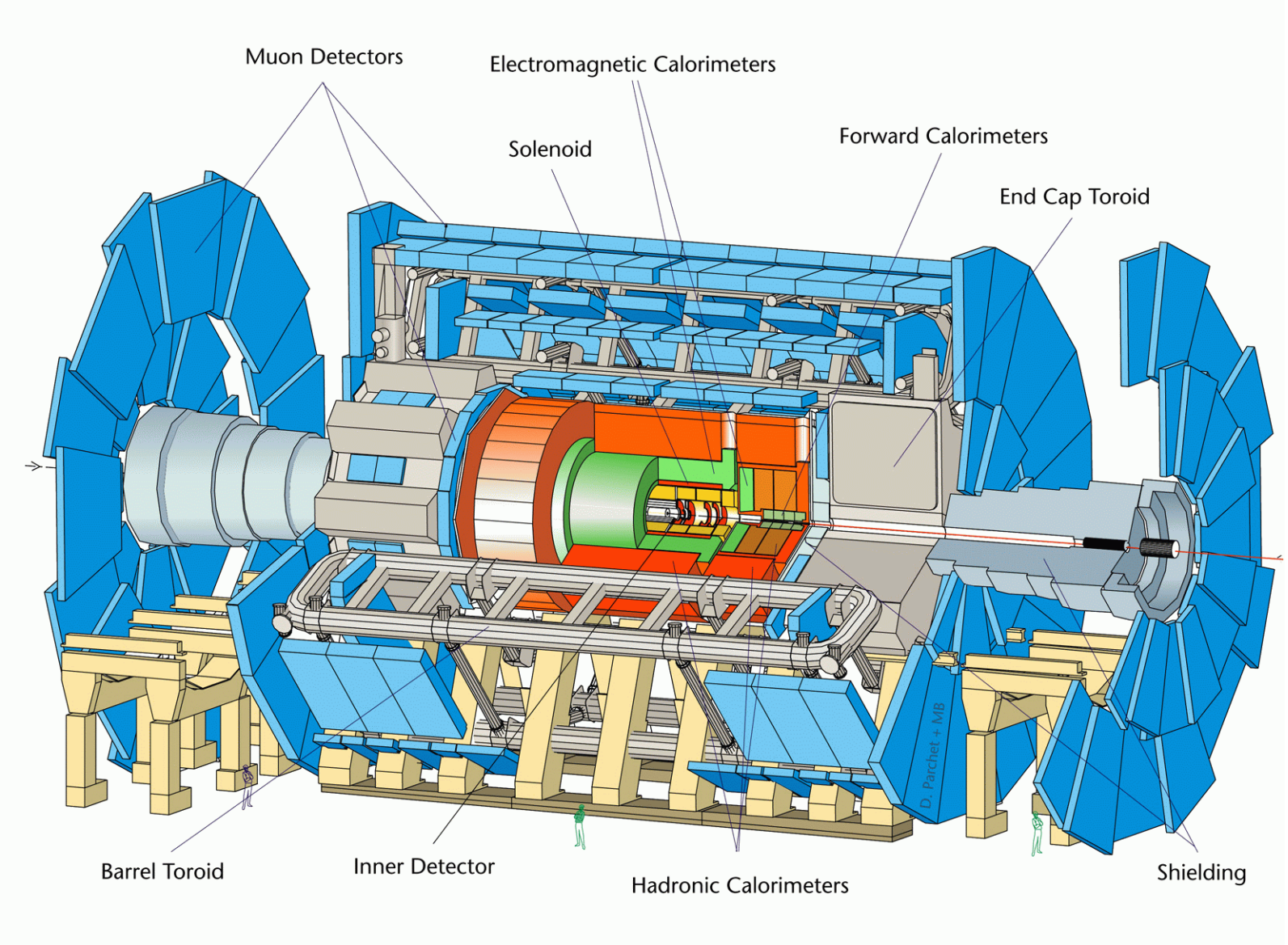
F. Zetti

Students/Interns

K. Copic, C. Flacco, J. Freeman, J. Haller, B. Jayatilaka, Y-H Kim, A. Ryan, Y. Wang

The ATLAS Detector

Very large, general purpose magnetic detector for the LHC:



The ATLAS Inner Detector:

Outermost system uses gas-filled 4mm straws

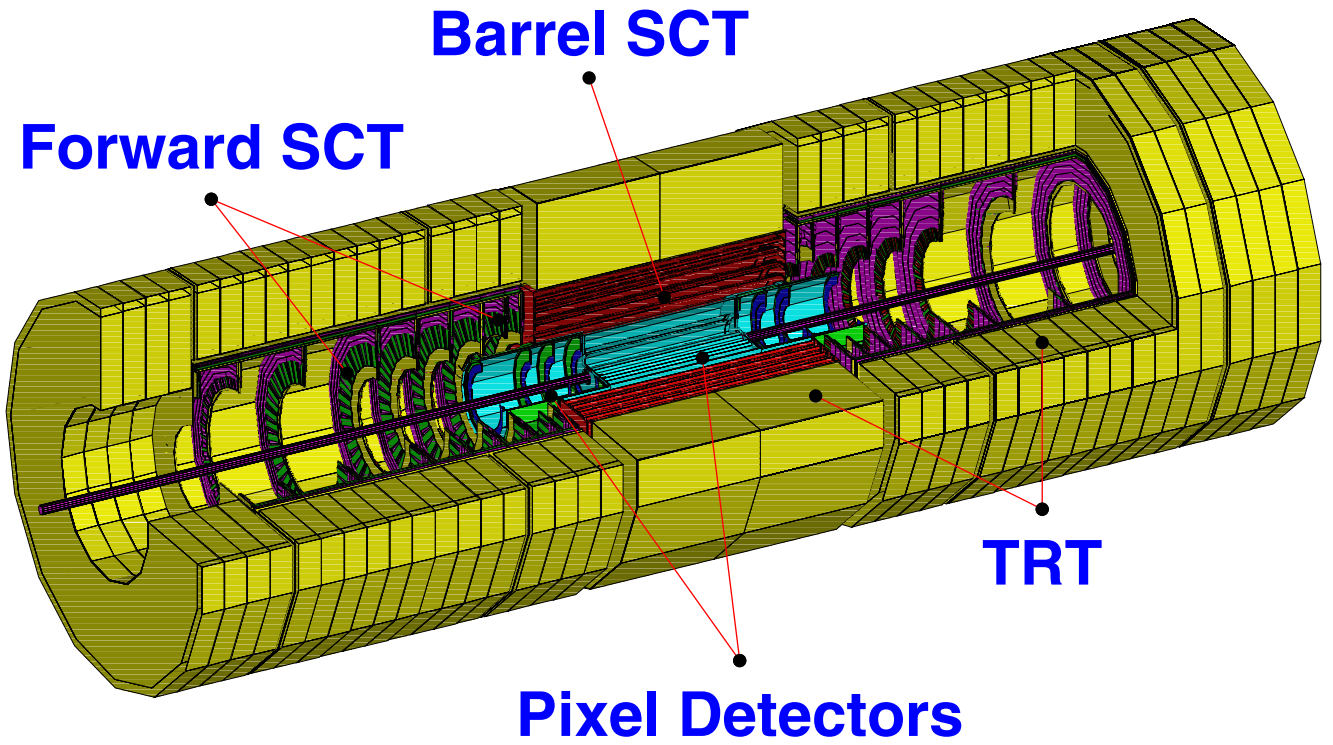
- There are 420K electronics channels, and a TR radiator supplies particle ID.

Intermediate radii contain a silicon strip tracker

- Four barrel layers and 9 disk layers contain 61 m^2 of silicon with 6.2M channels

Innermost system is pixel tracker

- Three barrel layers and 3 disk layers contain 1.8 m^2 of silicon and 85M channels



LBL Involvement in ATLAS

Silicon Strip detector:

- Development of production IC testing hardware
- Production and testing of roughly 700 barrel modules

Pixel detector:

- Development of on-detector electronics and test system hardware+software
- Module assembly prototyping, and production of roughly 300 pixel modules
- Local mechanics for disk
- Global mechanical support, support tube, and integration with beampipe
- Low mass services and integration with mechanics

Management of US ATLAS Silicon Activity

Computing and Offline Software:

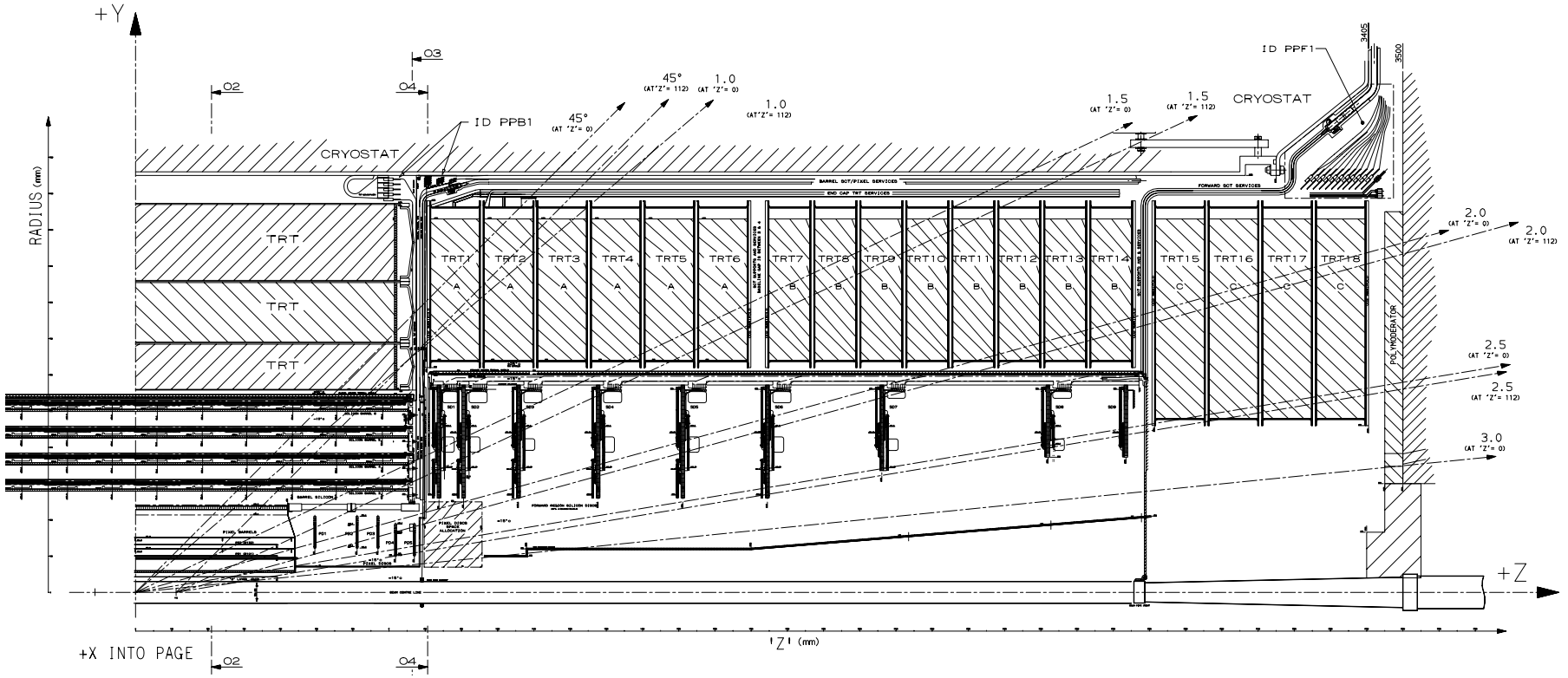
- Overall architecture of offline environment
- Software Framework to be used as backbone for all off-line software

Physics activities:

- Event Generators and Inner Detector simulation
- Analysis of observability of higher dimensions

SCT (Semiconductor Tracker) Activity

- Basic building block (module) is built from single-sided p+ on n sensors, bonded back to back to create double-sided modules with small angle stereo.
- System consists of about 4000 modules, arranged into 4 barrel layers and 9 disks on each end.
- Lifetime radiation dose is 10MRad worst case.
- LBL, collaborating with UC Santa Cruz, has concentrated on electronics and module construction.

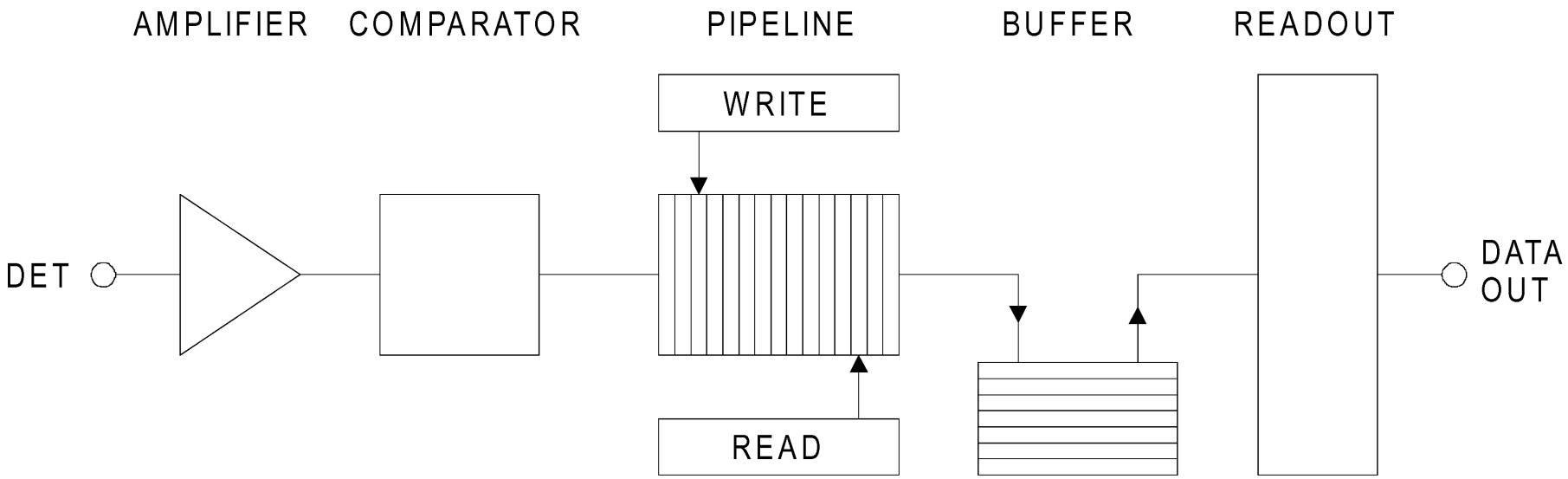


SCT Electronics

- ATLAS SCT readout is based on a binary scheme in which only the presence of a hit is recorded. This approach was pioneered in the US for SDC and ZEUS. Binary data is stored in a pipeline for L1 latency, zero-suppressed, and read out.

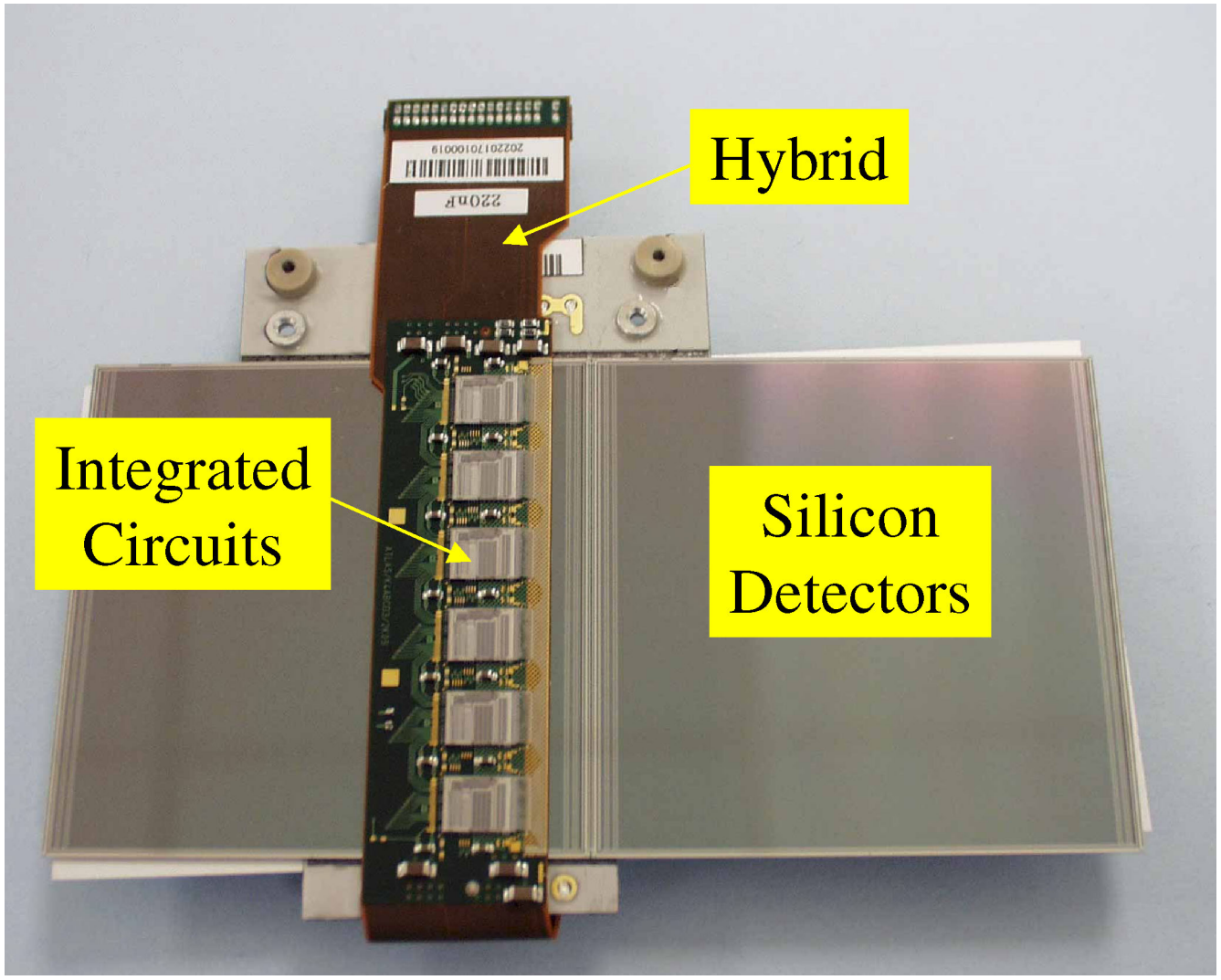
Two parallel developments were carried out:

- CAFE-M (bipolar analog front-end chip from MAXIM) and ABC (CMOS digital back-end chip from Honeywell)
- ABCD (BiCMOS combined design from ATMEL/DMILL).
- ABCD was selected. Pre-production wafers fabricated and being evaluated. ATLAS PRR in July, and then production should begin later this year.



SCT Modules

Modules are the building block of the SCT system:



Module consists of:

Four detectors precisely glued to a heat spreader. Small angle stereo implemented.

Hybrid package attached to the two sides of the module.

Approximate dimension is 6cm x 12cm active area.

- LBL effort has focussed on prototyping and precision tooling for module assembly

SCT IC Test System

LBL responsible for production wafer test system:

- Total wafer volume will be about 1000 wafers with target ATMEL/DMILL yields.
- Three production test sites planned: CERN, RAL, UCSC.
- High speed test system needed, with parametric test capability. Since DMILL chip performance will degrade significantly after 10MRad dose, chips must be tested beyond specifications to guarantee performance at end of lifetime.

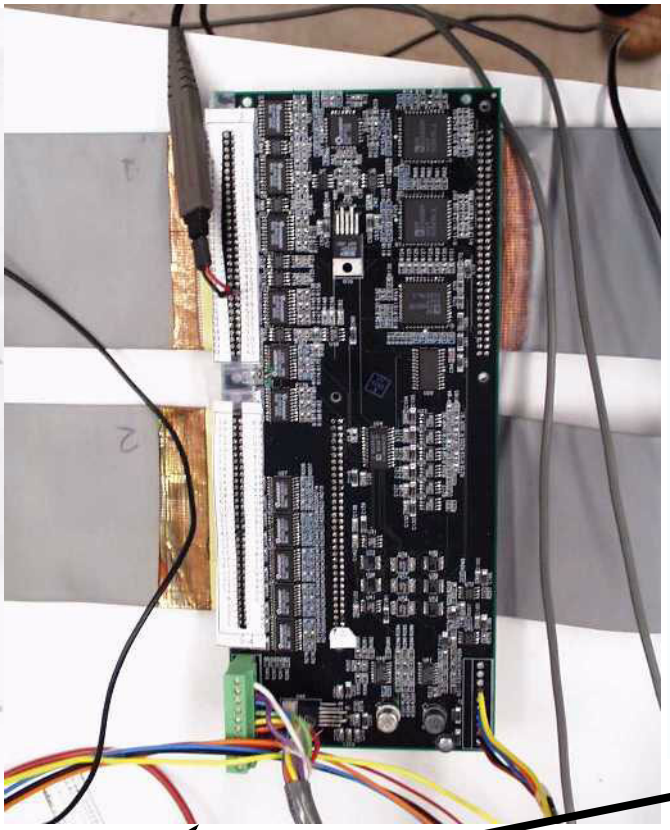
First systems were delivered to CERN, RAL, and UCSC earlier this year.

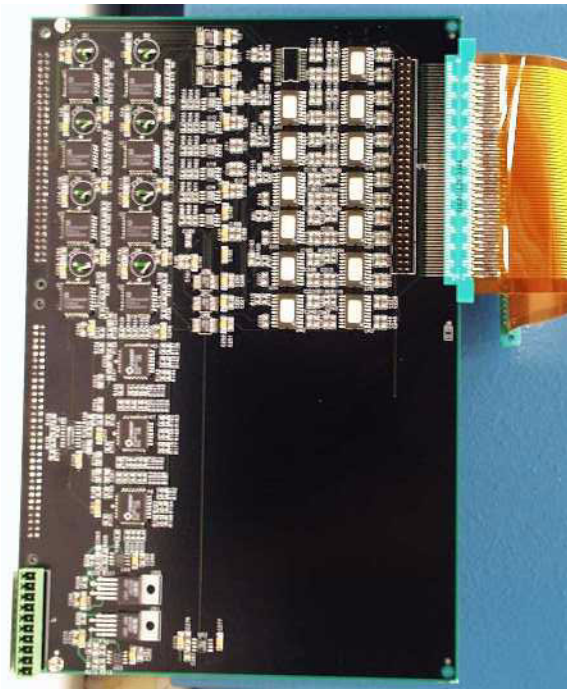
Correlation with results from old CERN system nearly completed.

Cross-check between systems at three sites being performed with set of 6 wafers.

Optimizing test sequences to achieve throughput of 1 wafer (250 die) in 6 hours. Can then test full production in 1 year.

- System consists of VME interface with intelligence in large FPGA, two high-speed control boards mounted closer to probe station, and custom probecard.

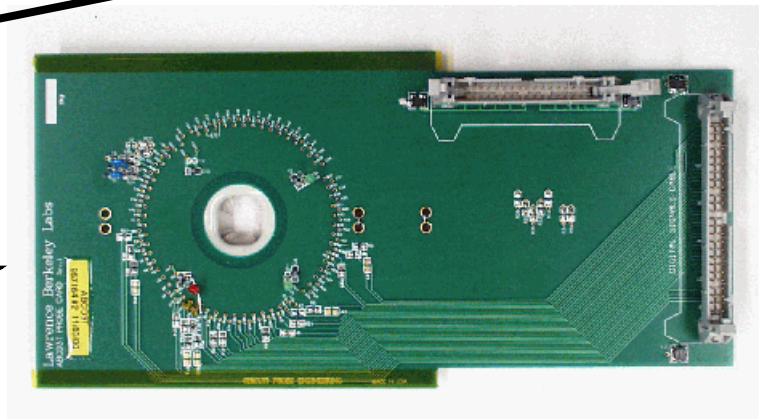




VME Interface

Digital and Analog Control Cards

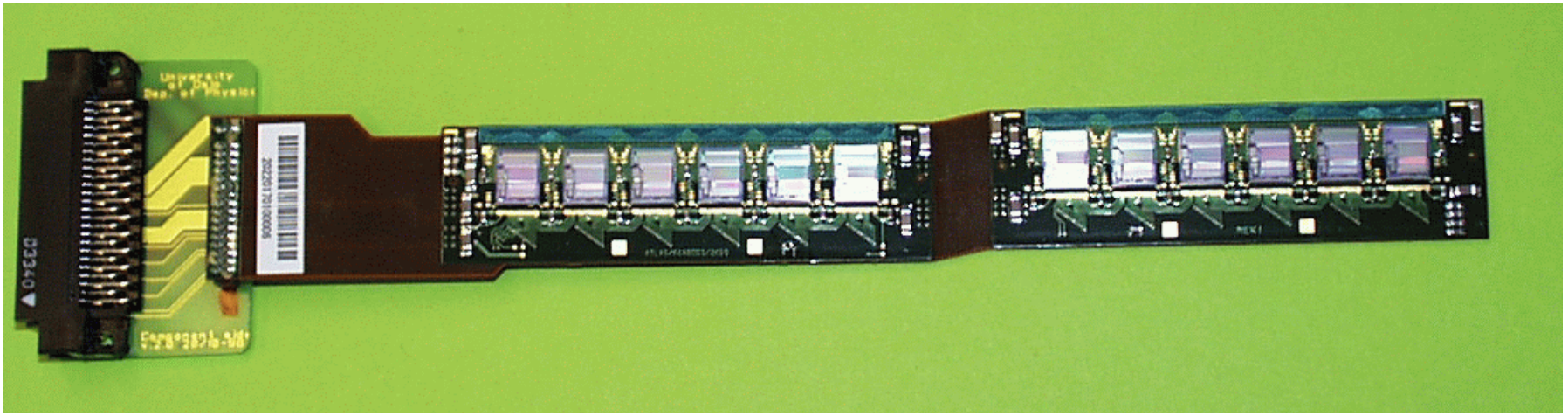
Probe Card



Silicon Strip Hybrid and Module Assembly

Responsibilities:

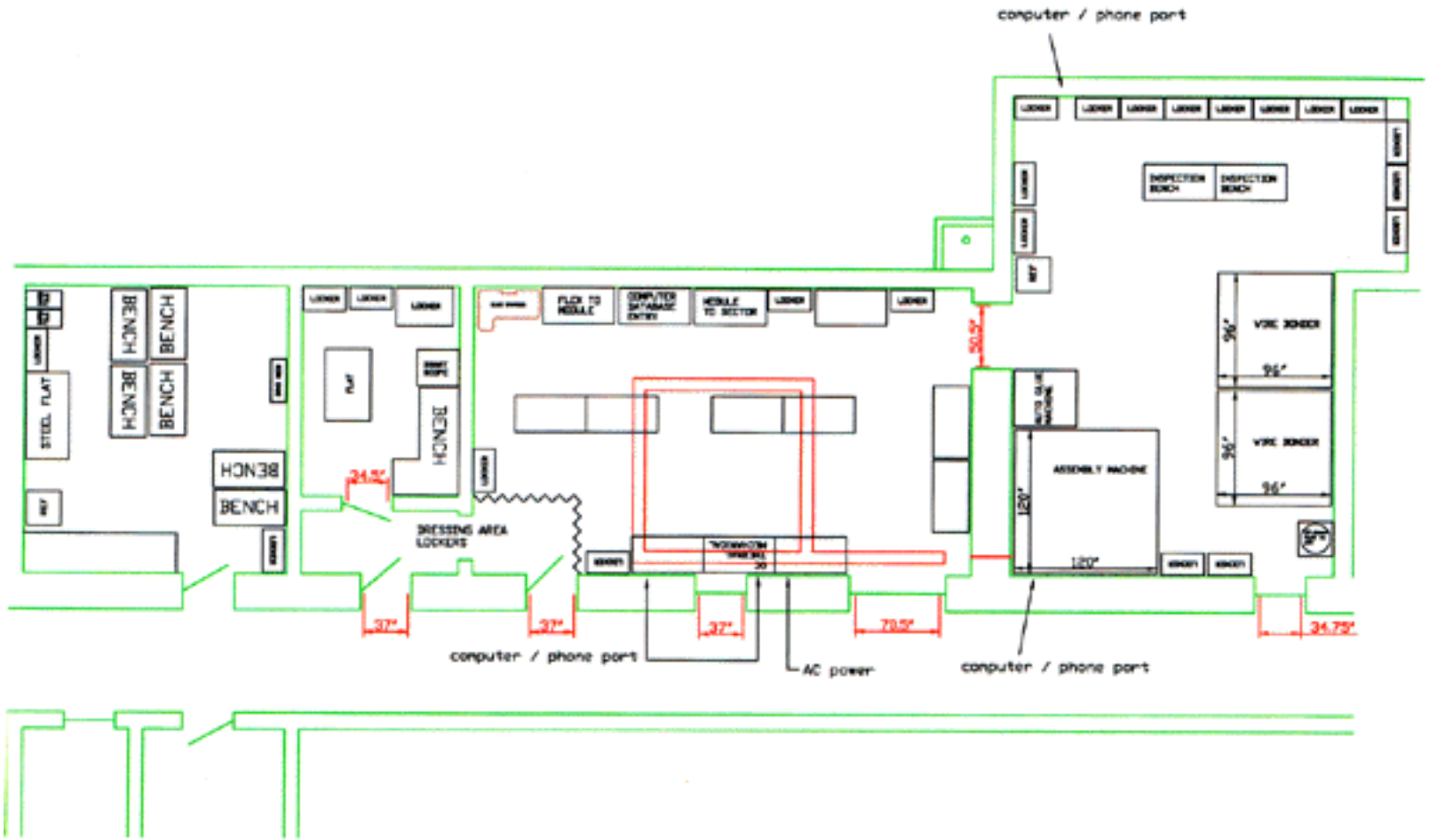
- Hybrids fabricated, passives loaded in Japan and delivered to LBL
- Hybrid die attach and wire-bonding to be performed in local firms and at LBL
- Hybrid testing and burn-in to be shared between LBL and Santa Cruz
- All module mechanical assembly to be done at LBL
- Module testing and burn-in to be done at LBL and Santa Cruz



- Barrel Module Final Design Review to take place at CERN next week.
- LBL to build several pre-production modules this Summer, then PRR in Fall.
- Production to begin in early 2002. Hybrid and Module assembly rate should reach 2-3/day, with production to take place over roughly 2 years.

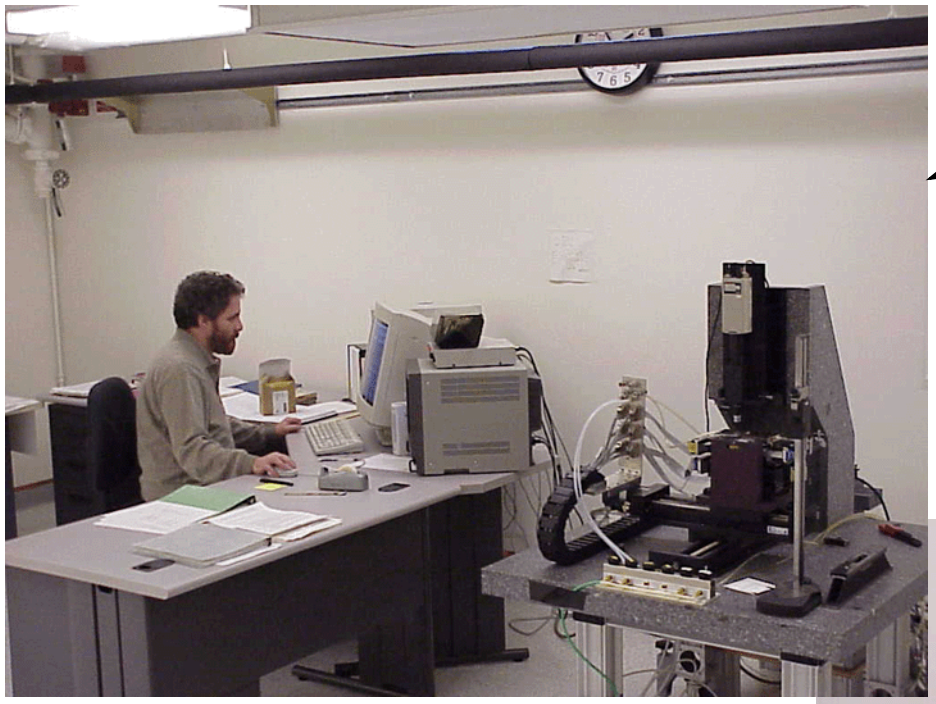
Module Assembly Space (SCT and Pixel)

- Thanks to support from LBL Directorate, significant space in Bldg 50 has been renovated into clean room space:



- Work begun in Late 99. Area is now equiped and functional.

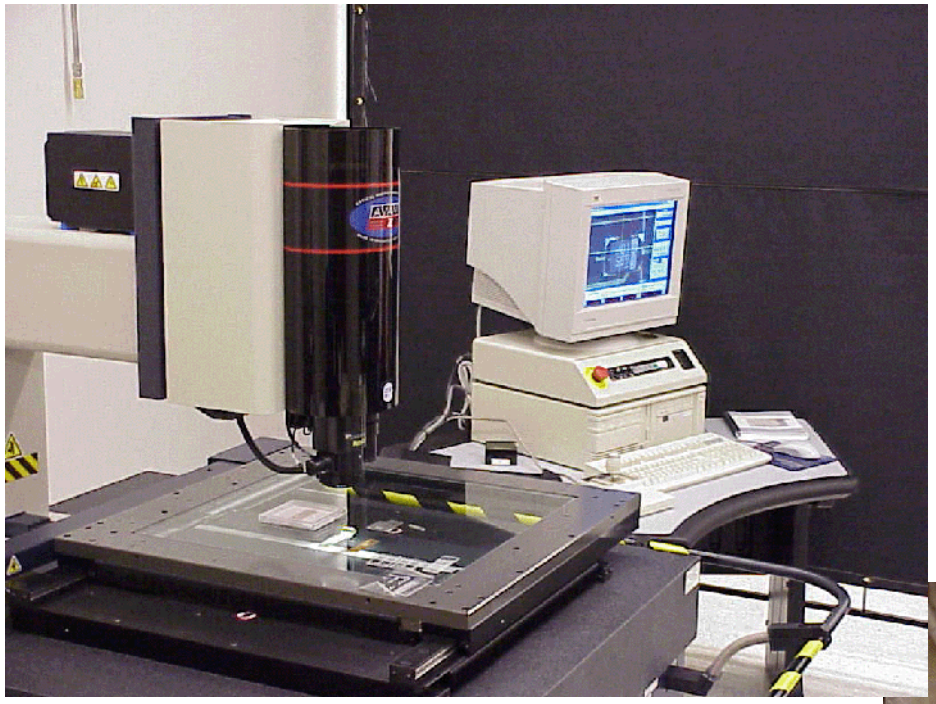
- Examples of equipment for strip module assembly:



Precision alignment and gluing station for assembly of SCT modules. Uses computer-vision assist to achieve tight mechanical tolerances.

Automatic wire-bonding machine used for bonding strip hybrids and modules, as well as pixel modules.

- Additional views of clean rooms:

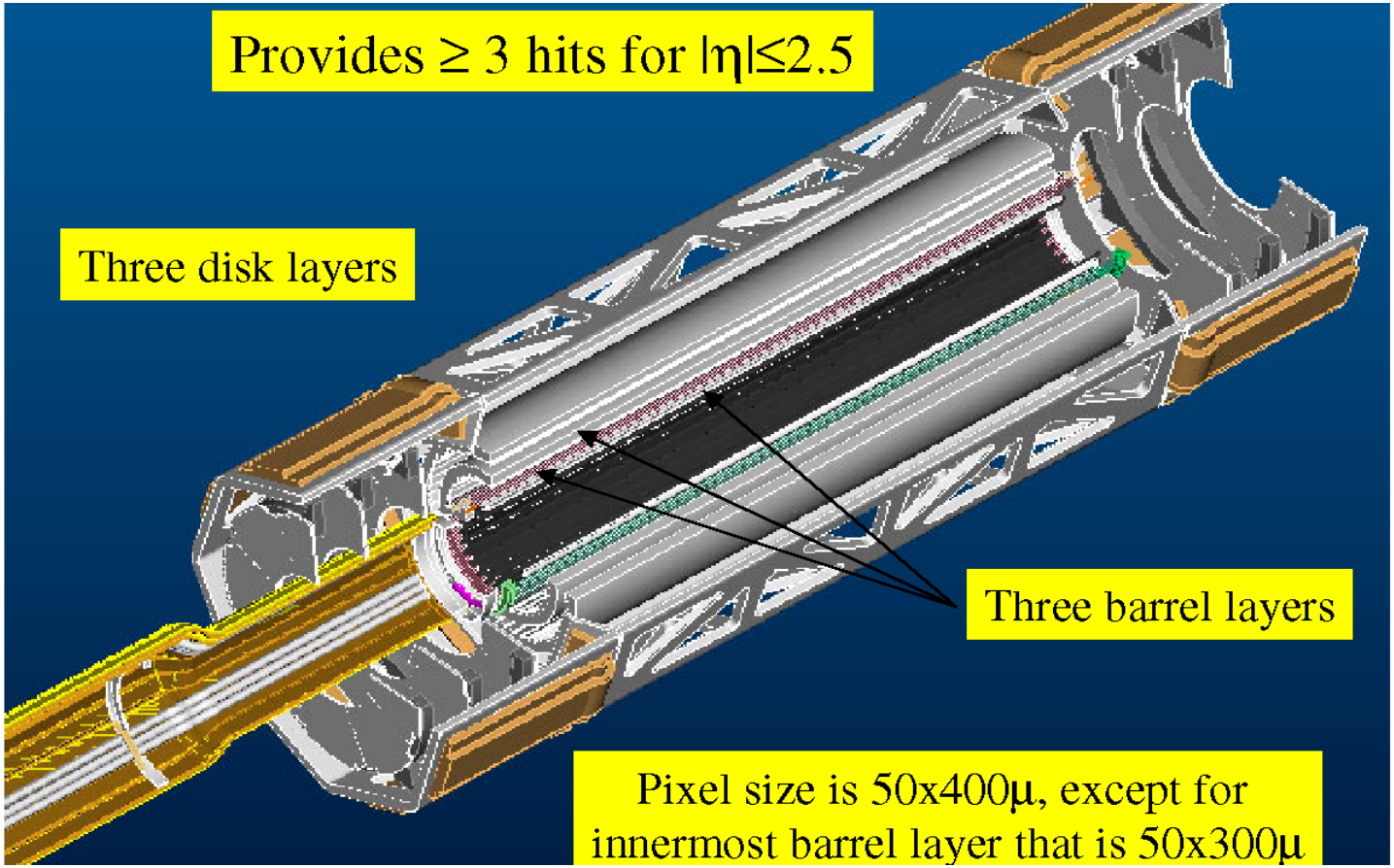


Coordinate Measurement machine (SmartScope) for use in optical survey of SCT modules and for Pixel module assembly and placement work.

View of larger of two rooms, with Pixel Module Assembly equipment beginning installation behind camera.

Pixel Tracker Overview

- LHC radiation levels prohibit operation of silicon strip detectors below radii of about 25cm. Lifetime dose for electronics is 30-50MRad.
- Small cell size (50μ x 300μ - 400μ) of pixel detector yields lower occupancy, better signal/noise ratio, and greater radiation tolerance.



- Physical size of system is roughly 1.6m long, with 0.2m radius. Innermost layer is at 5cm radius, and worst-case power consumption is about 4000A at 2V.

Significant recent events:

Pixel Baseline Review:

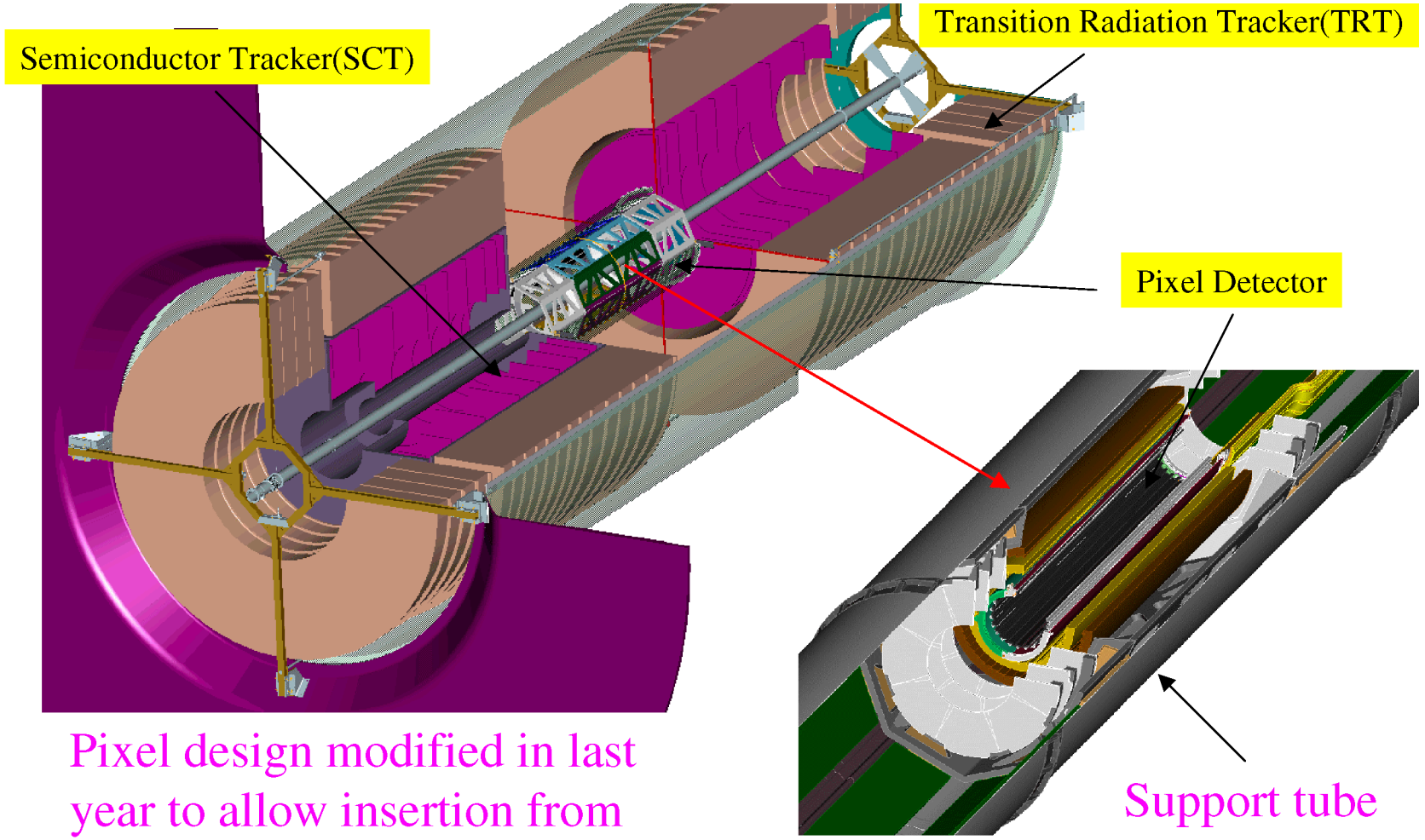
- US ATLAS Pixels has operated as an R&D project until this year. In Nov. 00, US ATLAS held a Baseline Review to decide whether to promote the US ATLAS Pixel effort to an official construction project.
- The outcome of this review was positive. The US baseline scope corresponds to a 2-hit system (2 disk layers and 2 barrel layers). This corresponds to the ATLAS Initial Detector configuration for first operation. The full 3-hit system is part of an upgrade proposal presently being formulated.

Deep submicron electronics effort

- In the past year, we have experienced a second failure of our first rad-hard vendor (ATMEL/DMILL) to manufacture our FE chip with acceptable yield, and a major cost increase from our second vendor (Honeywell). This left us with no viable, traditional solution to manufacturing our on-detector electronics.
- In parallel, we had begun investigations of converting our designs for fabrication using 0.25μ process and rad-tolerant layout techniques. This effort was ramped up to top priority in Sept 00, and should shortly be providing prototype chips.

Insertable Pixels:

- The failure of our two rad-hard vendors to produce viable electronics has led to major delays from our initial project schedule. In response, we have significantly modified the mechanical design and installation of the pixel detector to allow insertion of the complete system at the latest possible date:



Pixel design modified in last year to allow insertion from end of Inner Detector.

Pixel Mechanics

LBL now has the lead role in pixel mechanics in ATLAS

Responsibilities include:

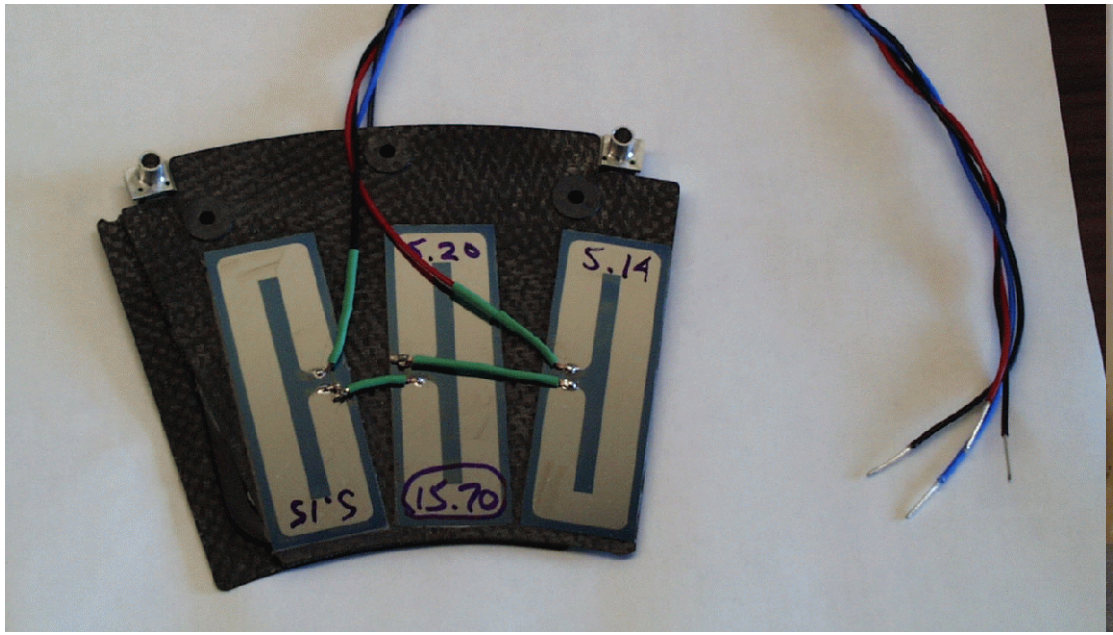
- Disk Structures
- Global Pixel Support Frame
- Support Tube
- Service Support Panels for power and cooling
- Other Items (low mass services, final assembly/installation) are shared with European collaborators
- Still other areas are not covered (Installation Tooling and others). The US could (and should) carry these, but funding is insufficient.

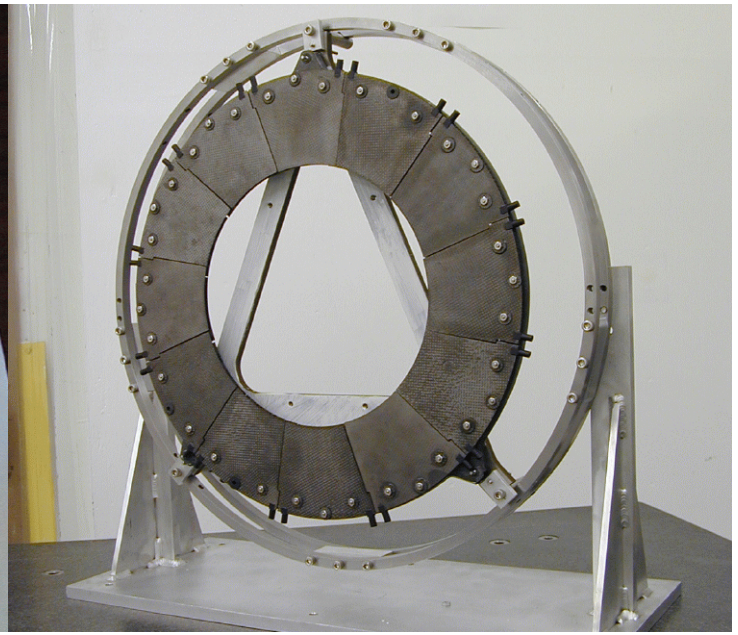
Schedule:

- The mechanics effort is quite mature, and will be starting production well before the electronics, in order to meet aggressive schedule.
- ATLAS PRR (Production Readiness Review) for Local Support structures and CDR (Conceptual Design Review) for Global Support structure in July.
- Production of first elements (disk sectors) is planned to begin in July 01.

Disk Structures

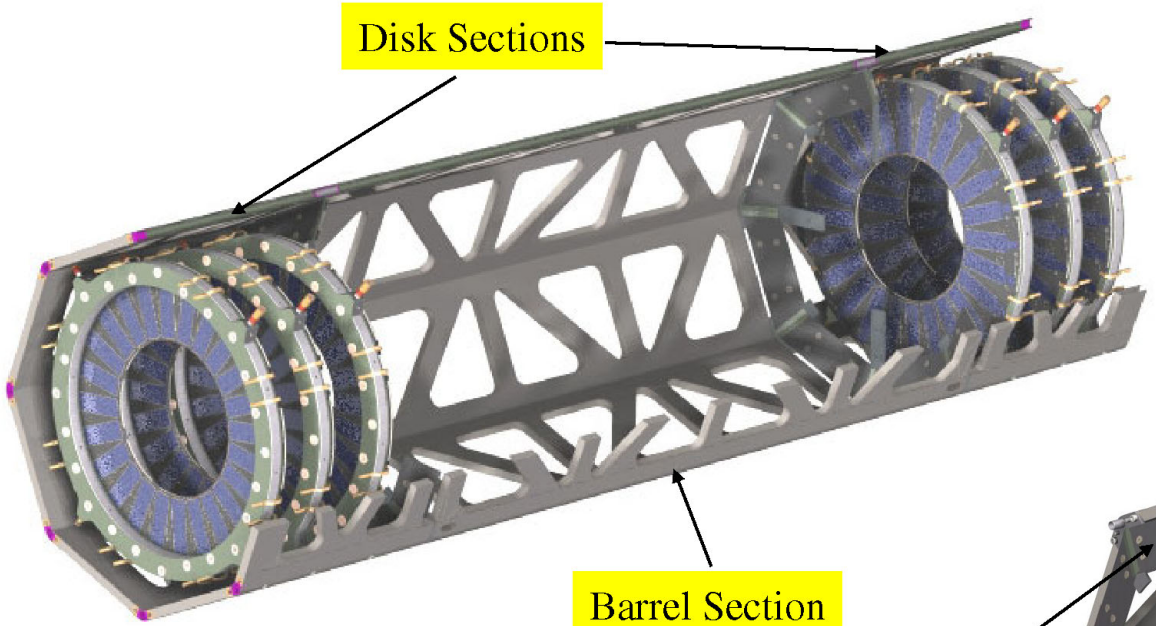
- Disks are composed of 8 Sectors that provide mechanical support and cooling, and Support Rings onto which the Sectors are mounted.
- Six modules are mounted on each sector, three on each side. Full coverage is achieved by displacing modules on one side by module half-width.
- Sectors are attached to Support Ring at their outer radius only. Support Ring is attached directly to Global Support frame.
- Sector design consists of thin Carbon-Carbon plates separated by low-mass filler, and thin-wall Al cooling pipes (evaporative C3F8 cooling used).
- Extensively prototyped. Sectors are ready to begin production in July. Final design of Support Rings is complete, and design of fabrication tooling is starting.

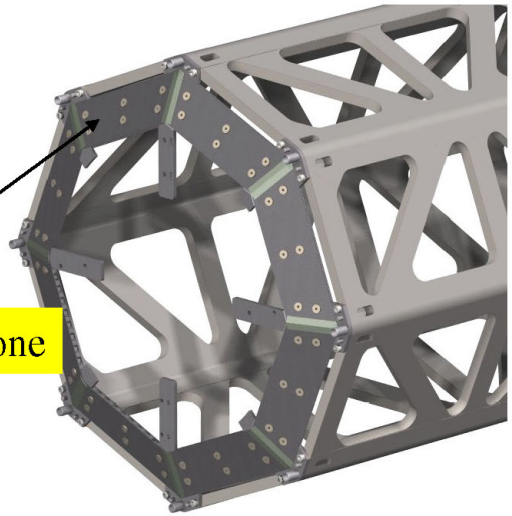




Global Pixel Support Frame

- Ultra-stable, low mass structure which must provide integrated support and cooling for more than 10kW. Coolant temperature is -25C.
- Support Rings for disks, and Support Shells for barrel provide intermediate support for Local Supports (Sectors and Staves).
- Major integration task to integrate power/signal cabling and coolant connections.

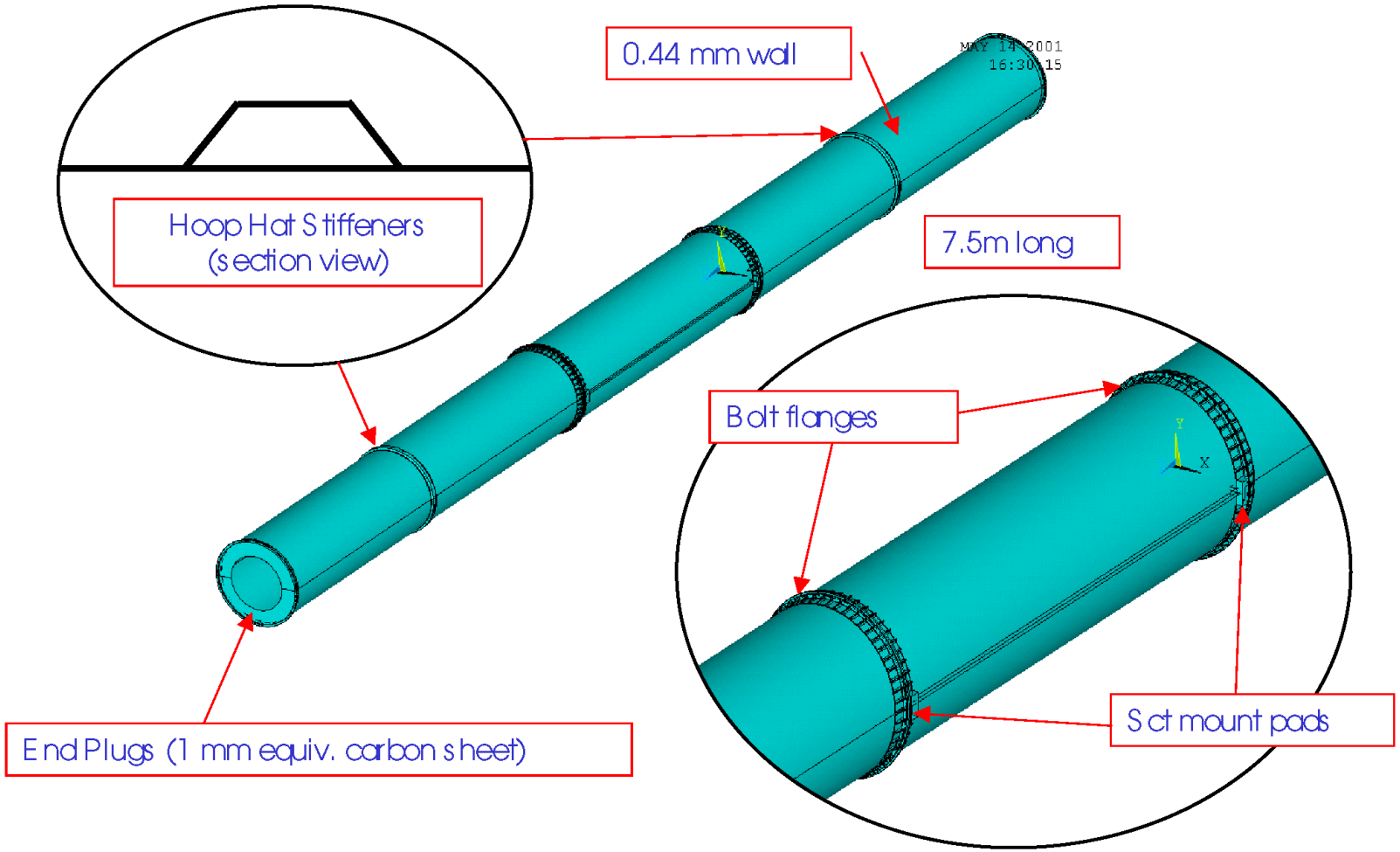




- Frame design advanced.
- Support cone prototype complete next month
- Trial insertion of disk ring into prototype of frame started

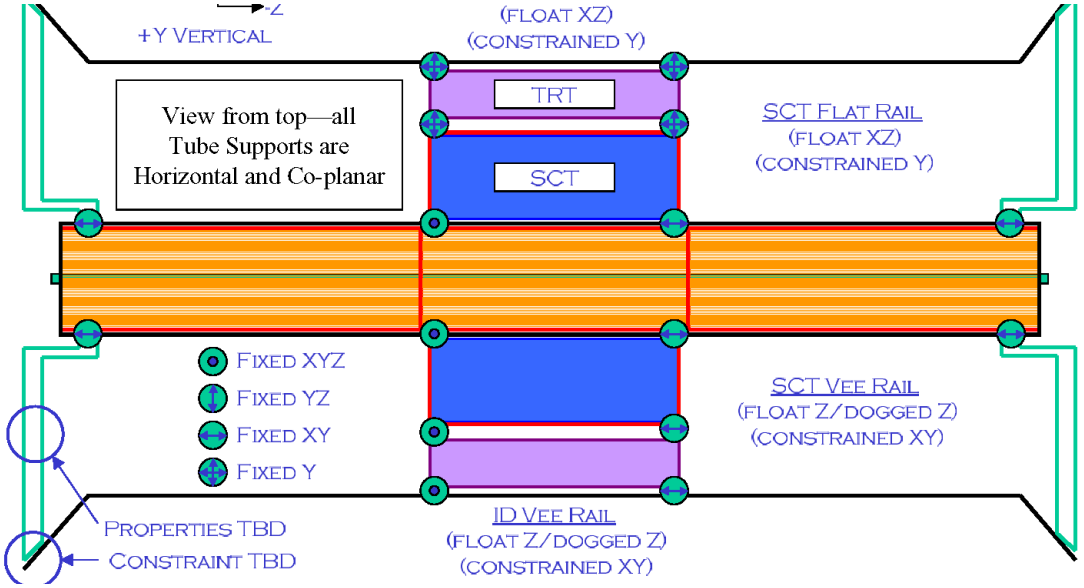
Support Tube

- Three piece composite structure with integrated rails to support Pixel Detector and Service Panels. Beam pipe is now integrated with/supported by this tube.
- First version of design complete, undergoing static and dynamic FEA analysis. Critical to control vibrational properties to preserve pixel alignment:

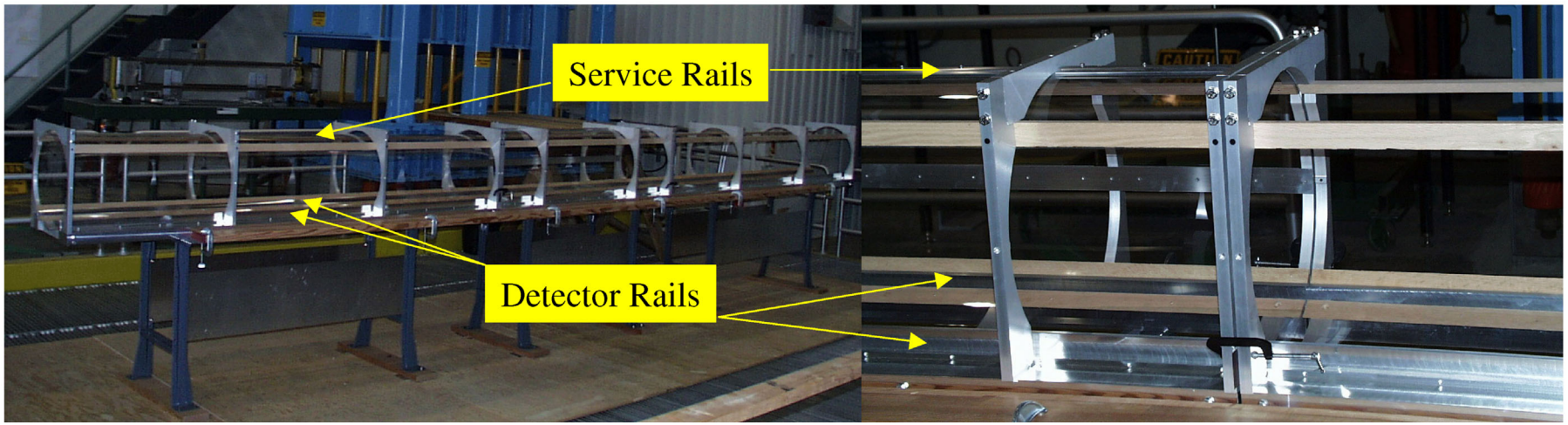


Support Tube is complex integration problem:

Pixel Detector services integrated inside, complex support conditions in ATLAS ID:



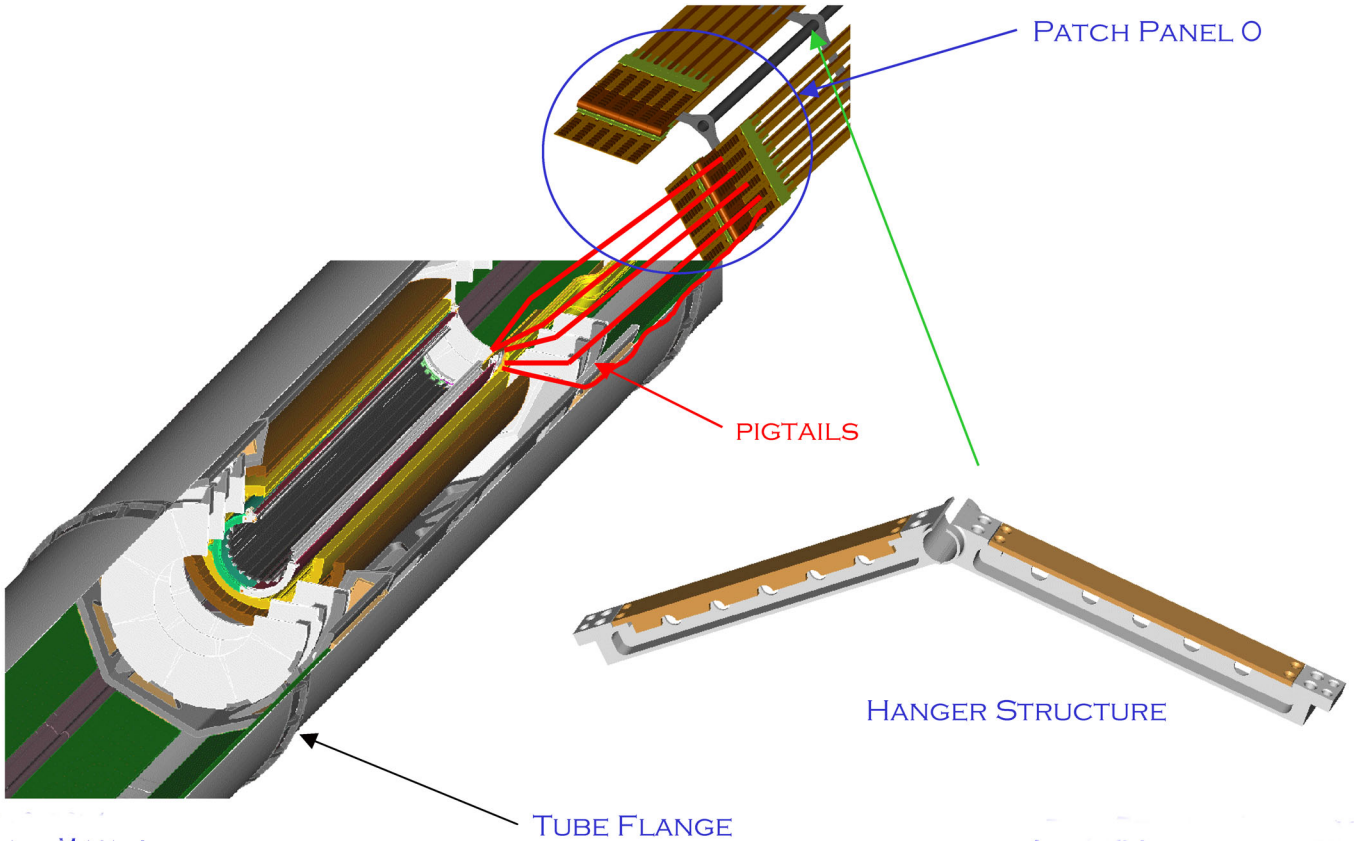
Constructing a complete mockup (in old Bevatron) to understand and practice assembly and installation sequence, and iterate design if necessary:

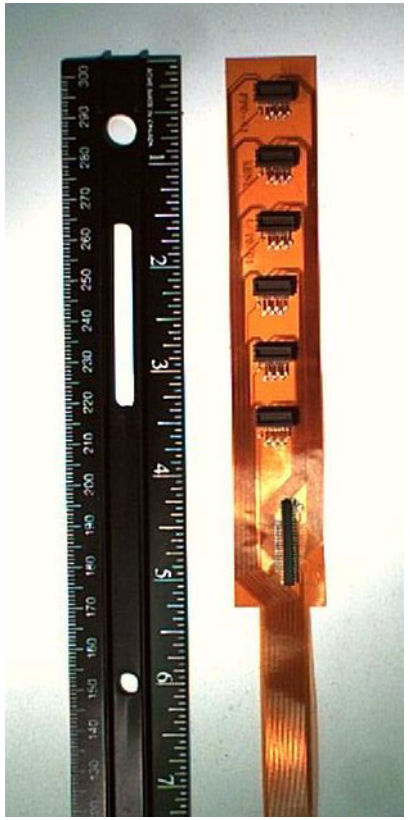


Service Support Panels for power and cooling

Integration of low mass services is complex:

- Present baseline calls for possible in-situ installation of B-layer with no vacuum break. This requires accessible services on both ends of Global Support Tube.
- Concept involves panels integrating LV, HV, optical, and cooling plant together. Panels slide along rails inside Support Tube. First prototypes of PP0 have already been built as Flex circuit with many folds to achieve 3m length.

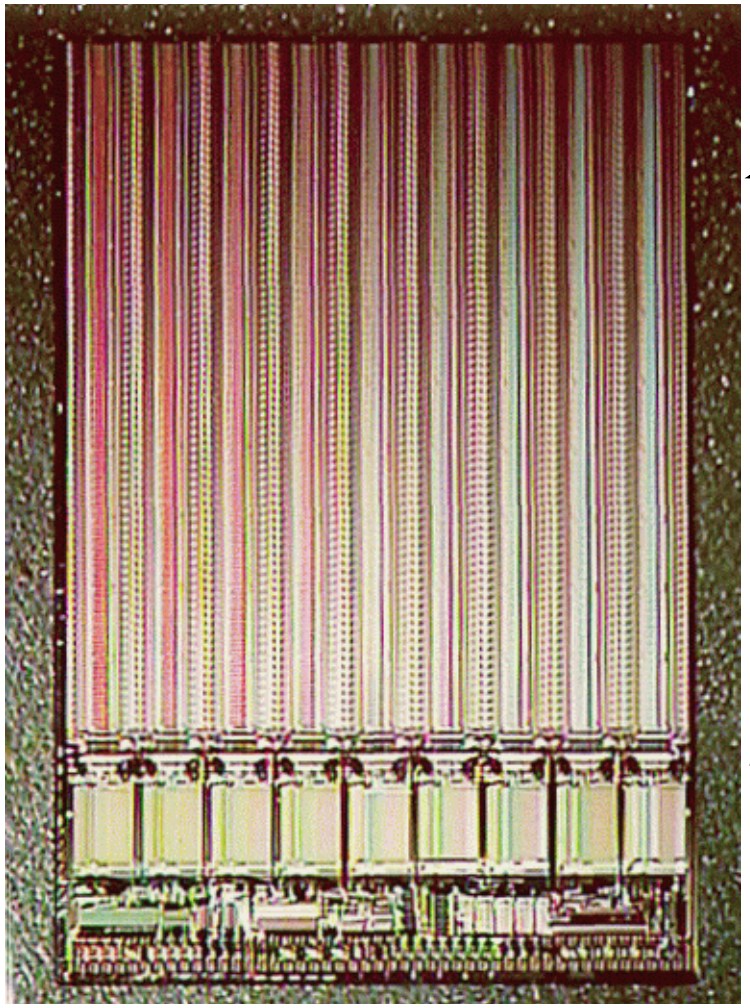




Pixel Electronics

LBL has a leading role in the pixel on-detector electronics:

- First complete pixel FE chip prototypes produced in 98 (LBL design). Used for extensive lab and testbeam studies in 98/99, validating basic performance goals.



Active matrix of 18x160 pixels, each 50μ x 400μ.

Die size of 7.4mm x 11.0mm

Inactive region containing buffering, control, and all housekeeping functions.

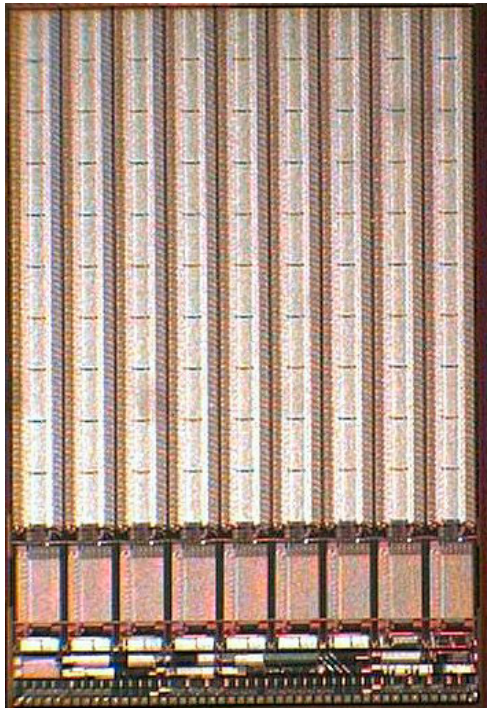
Final version has less than 30 bondable pads at bottom. Very high level of integration.

Must be active to three edges.

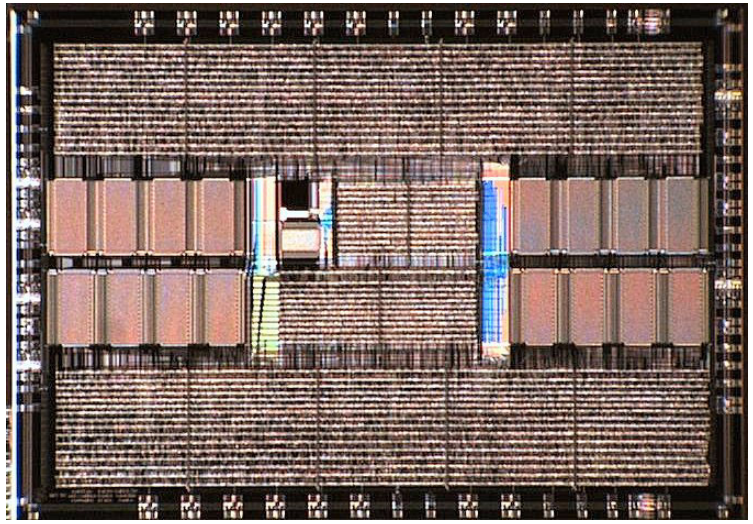
- LBL has lead in FE chip design, and does overall electronics coordination.

Complete on-detector electronics consists of four chips:

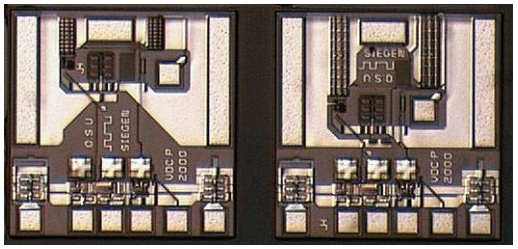
- FE chip described above, 16 of which are used for a module
- MCC (module controller chip) performs event building on 16 FE chip data streams, and other module housekeeping functions, providing 3-wire interface to module (data in, data out, clock). Synthesized design, developed by Genova.
- Opto-chips: VDC (VCSEL Driver Chip) to drive data off-detector, and DORIC to decode encoded clock/control stream. A joint development of OSU and Siegen.
- Recent engineering runs all have complete chipset (DMILL chips shown here).

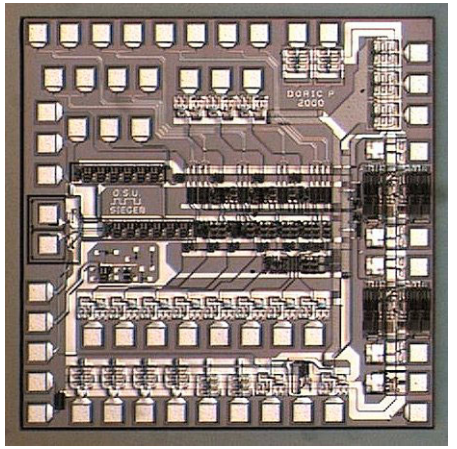


FE-D2



MCC-D2

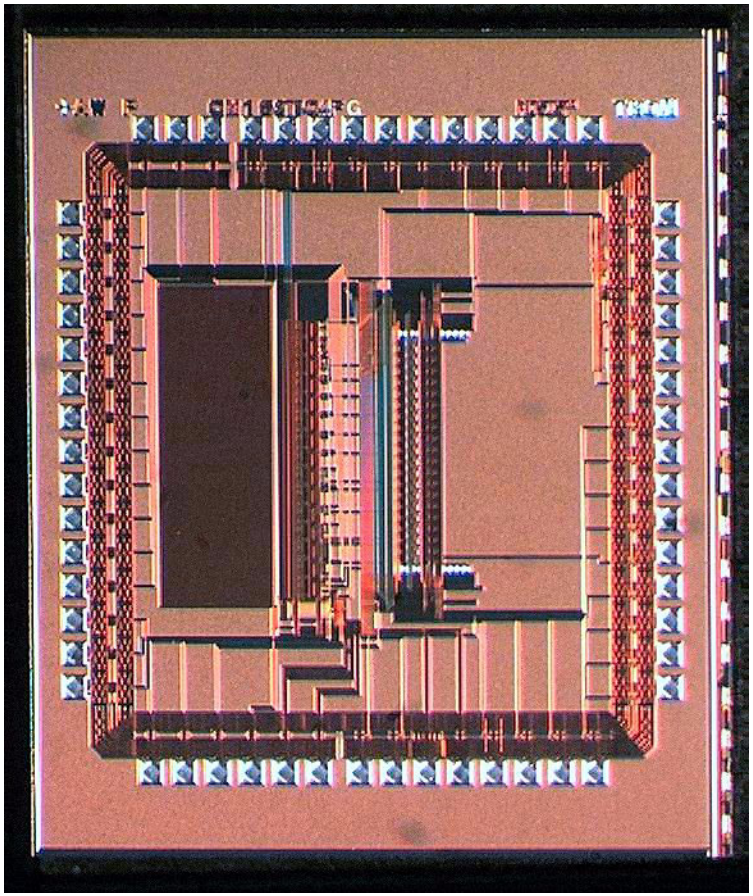




DORIC and VDC

Progress towards 0.25μ Pixel FE chip

- Adopted dual process approach (TSMC/IBM) to provide prototyping and production flexibility. Production likely to be IBM, due to CERN Frame Contract.
- Submitted first digital test chip to TSMC in Jan 01. Limited functionality, but it works roughly as expected.
- Submitted serious Analog Test chip to both IBM and TSMC in Feb/Mar 01. TSMC chip arrived last week.



Chip contains roughly final designs and layout for all required analog blocks.

It contains 20 pixels and their control logic, plus load capacitors and leakage injection capability.

It contains 15 8-bit DACs and an internal reference, providing complete stand-alone (no analog inputs) adjustment of all analog bias currents.

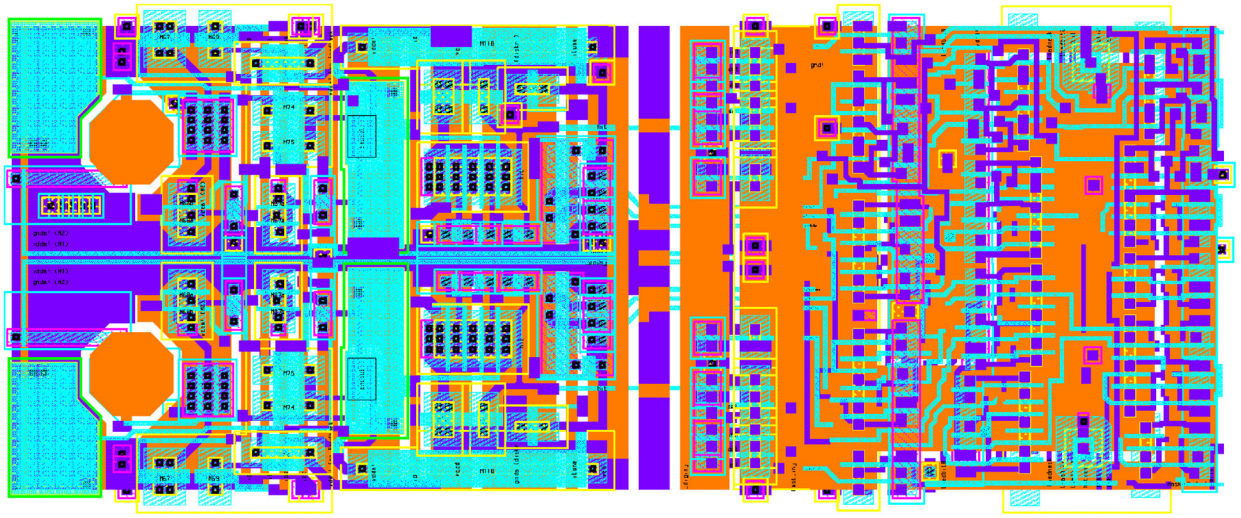
Contains prototypes of critical differential I/O circuits as well.

Conservatively designed to operate below 2V to improve lifetime and reduce risks from overvoltages.

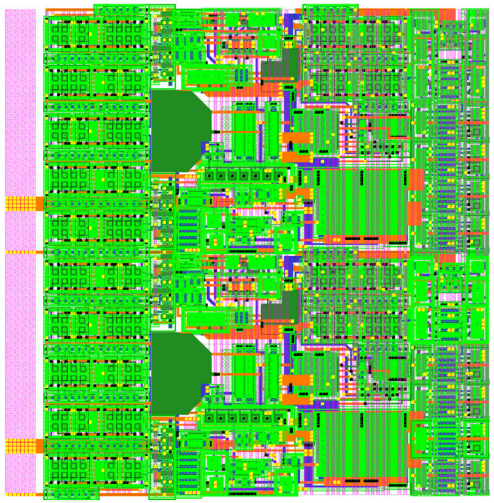
Presently integrating complete FE chip:

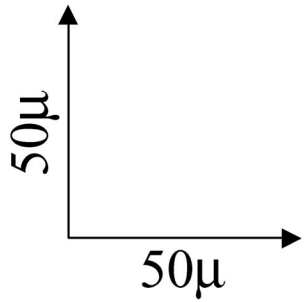
- Comparison of designs in DMILL and 0.25µ:

Two pixels (analog) in *DMILL*



Two pixels in 0.25µ





- New 0.25µ design has significant additional functionality, including dual 5-bit trim DACs, a two stage front-end, and a differential back-end.

New 0.25μ design improvements:

- Replaced 3T DRAM cell with 8T differential SRAM cell. Timestamp inputs to pixel and data/address outputs are now fully differential for reduced noise and increased speed.
- Moved TOT calculation function from bottom of chip to bottom of column, allowing simple digital timewalk correction (charges below given threshold are shifted by 25ns), and filtering of low TOT hits if desired.
- Increased EOC buffering per column pair from 24 in DMILL (marginally OK for outer pixel layers) to 40/64 in 0.25μ, which is more than adequate for B-layer occupancies.
- Integrated all analog functions tightly to bottom of column to improve noise immunity.
- Using extensive automatic place and route tools for logic blocks in pixel, end of column, and bottom of chip, to reduce layout time and focus layout effort on critical storage blocks.
- Included all SEU-tolerant FF for configuration information (14 bits per pixel, plus roughly 200 bits at bottom of chip), so do not expect problems with bit-flips. Also, carefully analyzed all state machines for bit-flip impacts, and there should be only transient effects.
- Using more sophisticated power and timing analysis tools to optimize the performance of the design.

Near Term Goals

- Test Analog Test chip from both TSMC and IBM, irradiate at LBL 88" Cyclotron and CERN PS during next 2 months.
- Submit complete engineering run (12 200mm wafers) by end July. This run will contain pixel FE chip, MCC chip, opto-chips (VDC and DORIC), and several minor test chips. It will provide a complete 0.25μ chipset for pixel prototyping, startign in Fall 01, and continuing into the first half of 2002.
- After complete lab and testbeam characterization of these chips, including irradiation of complete pixel modules, expect to submit a second version of these chips in mid-2002.
- Production should begin in 2003. Intend to deliver complete 2-hit system for installation into ATLAS by end 2005.

Longer Term Goals:

- The performance of the pixel B-layer largely determines the impact parameter resolution of the tracker. Therefore, it is critical for this layer to work perfectly, and the ATLAS physics reach depends strongly on its capabilities.
- Expect that this layer will be upgraded whenever the technology will allow a significant performance increment.
- It is also possible that we have underestimated the occupancies that will be encountered at 10^{34} luminosity, and better performance will be needed.
- We are already working with the next generation CMOS process from TSMC (0.18μ), which would allow further improvements in pixel size, and FE chip functionality. By the time of an upgrade to the B-layer, we would likely be working with 0.13μ process with 8 metal layers (MOSIS availability early 2004 ?).
- There are many technical issues to address, including radiation hardness and lifetime issues (thinner gate oxide could lead to Gate Rupture events, Hot Carrier effects increase, basic ingredients like gate oxide could change).
- There are also many design issues to address, particularly in the analog area. It becomes more difficult to do analog design with reduced ratio of supply voltage to device VT, and leakage effects in very thin oxides become significant.
- In order to be on the knowledge and experience path to carry out a B-layer upgrade, R&D needs to start as soon as the production chips are launched.

Irradiation Capabilities at LBL

LBL 88” Cyclotron is very useful for CMOS irradiations:

- Has been used to characterize DMILL chips earlier this year. CERN PS typically available only form May to Nov each year, so LBL capability can be critical.
- We plan to irradiate our TSMC/IBM Analog Test chips at the Cyclotron. This will provide us critical feedback before submission, before data from CERN PS:

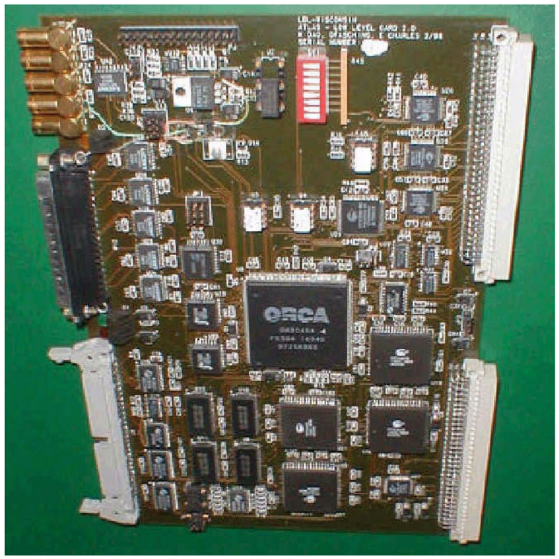
FE-D2S being tested at 88” Cyclotron using N_2 coldbox to irradiate at about -5 C.

Energy of 55 MeV is fine for total dose, and adequate for SEU studies.

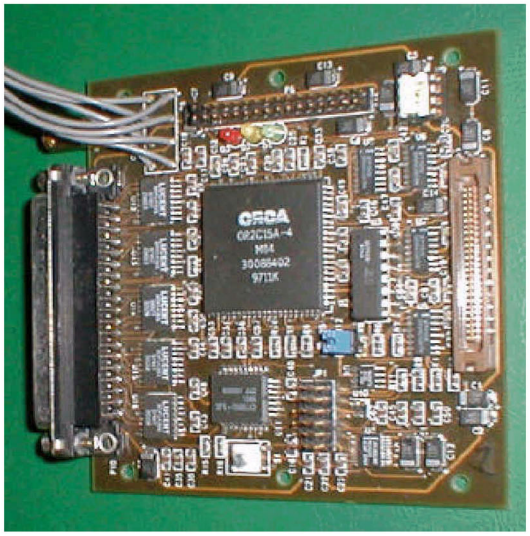
Electronics Test System

- LBL/Wisconsin developed original test system in 97/98. This system has been used for all wafer probing, and characterizing of single chips and modules in the lab and the testbeam. There are 16 systems distributed throughout ATLAS. A common test system has been critical for progress in electronics and modules.

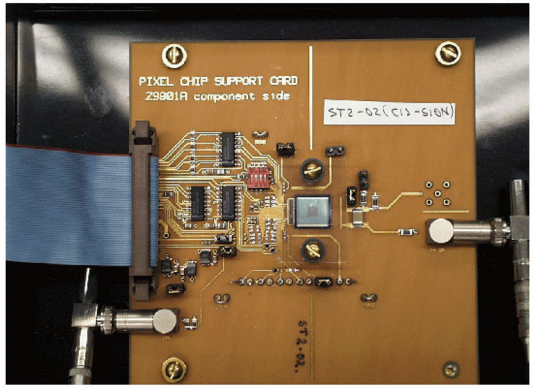
Components of Current Test System:

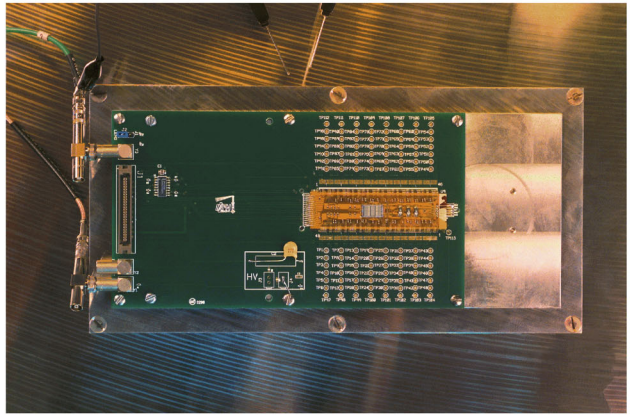


PLL

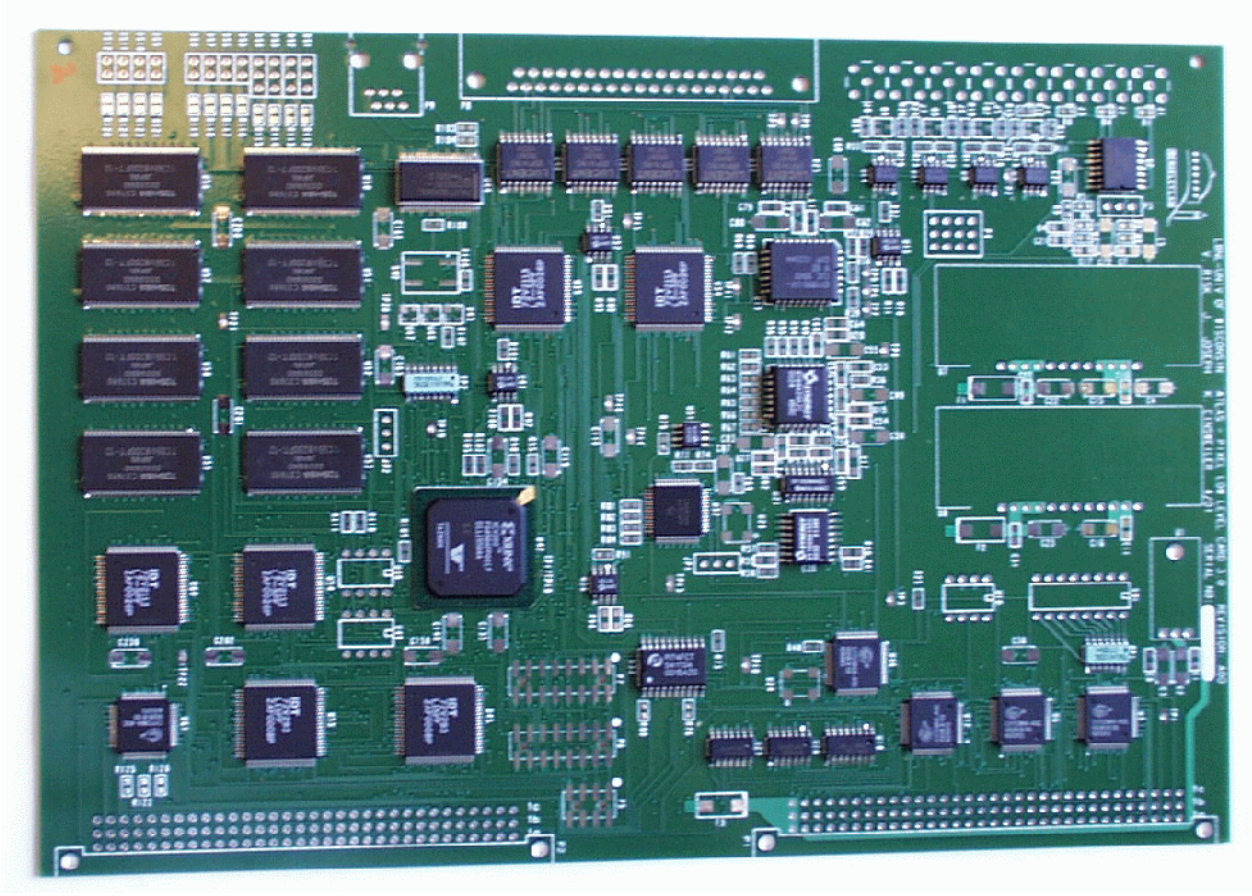


PCC





- Second generation now designed and starting fabrication. Incorporates experience from present system, and is optimized to cover full scope of production needs with one modular set of hardware. This spans the range from wafer probing, to lab and testbeam characterization, to production module testing and burn-in.
- Includes upgrades to test capability, including variable clock frequency, variable amplitude and phasing of critical input signals, and optimized buffering.



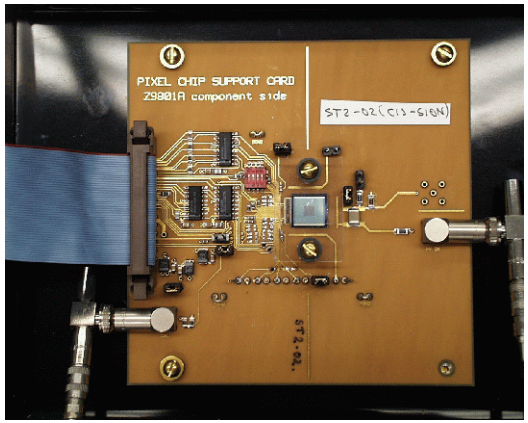
New VME card being loaded now for testing.

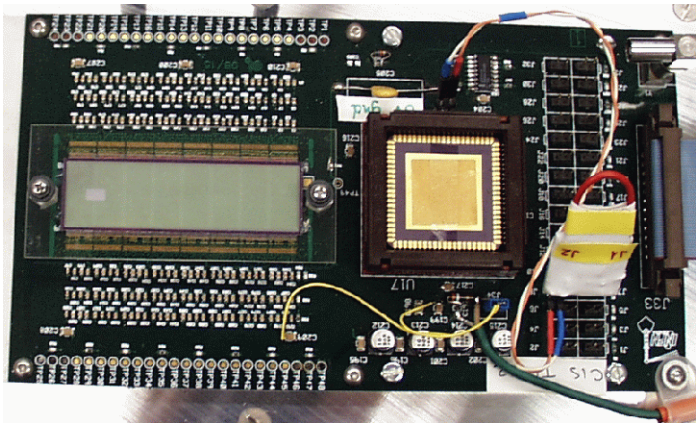
Includes factor 8 increase in on-board RAM (complete characterization of up to 64K pixel modules), factor 10 in FPGA gate count, and factor 8 in critical FIFO's needed for high speed operation.

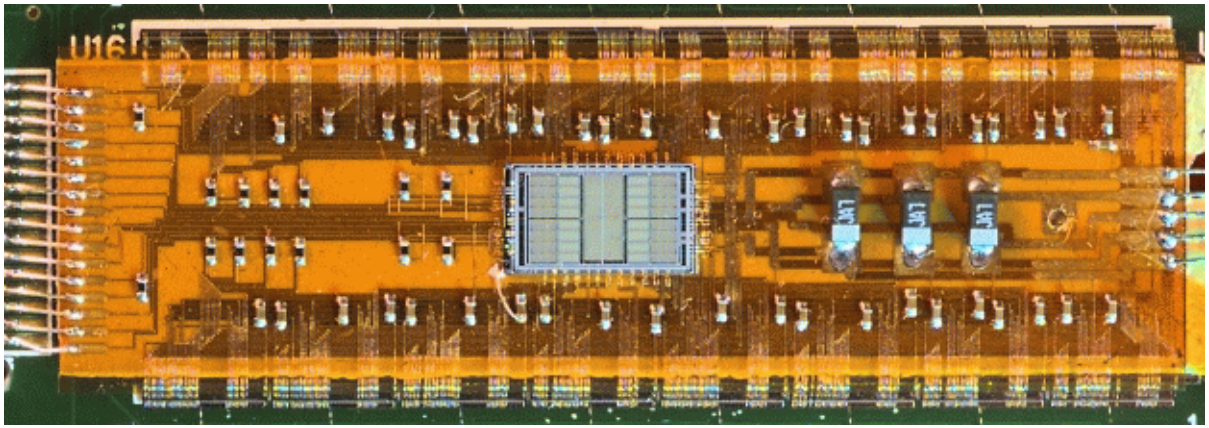
Pixel Modules

LBL has major role in Module Prototyping and Assembly

- Built many “single chip” devices using smaller sensors for small-scale studies. Some studies were done with irradiated sensors and rad-soft electronics.
- Built about 10 modules with IZM solder bumps, several as “bare” modules with interconnections on PC board, several as “Flex” modules, others as “MCM-D” modules. Some, but not all, of these modules work very well.



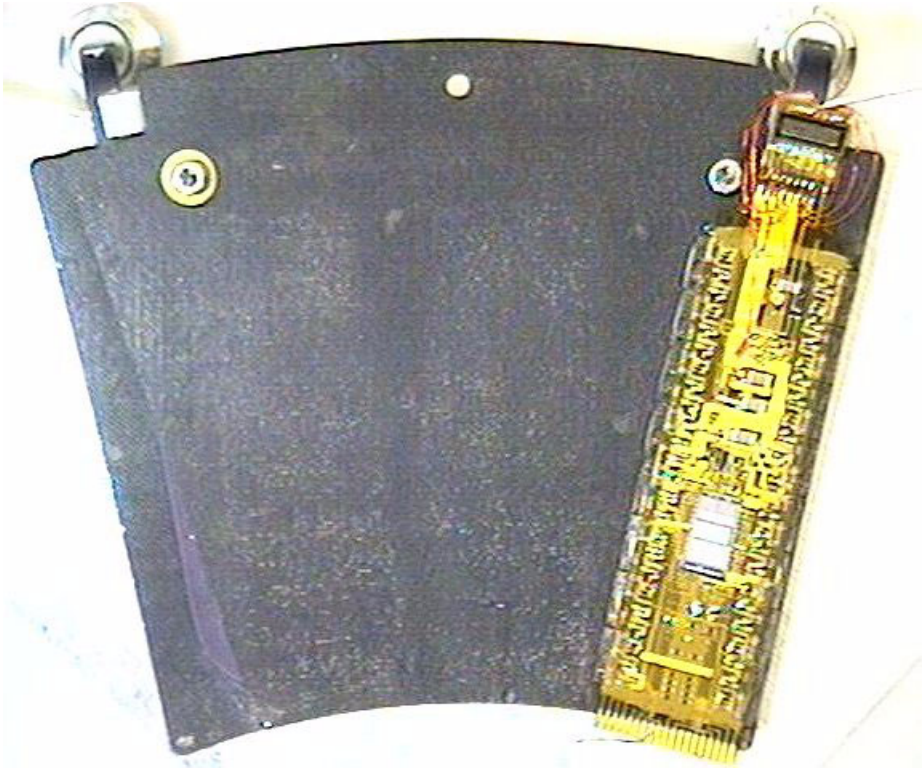




Next Steps in Module Prototyping

Real modules:

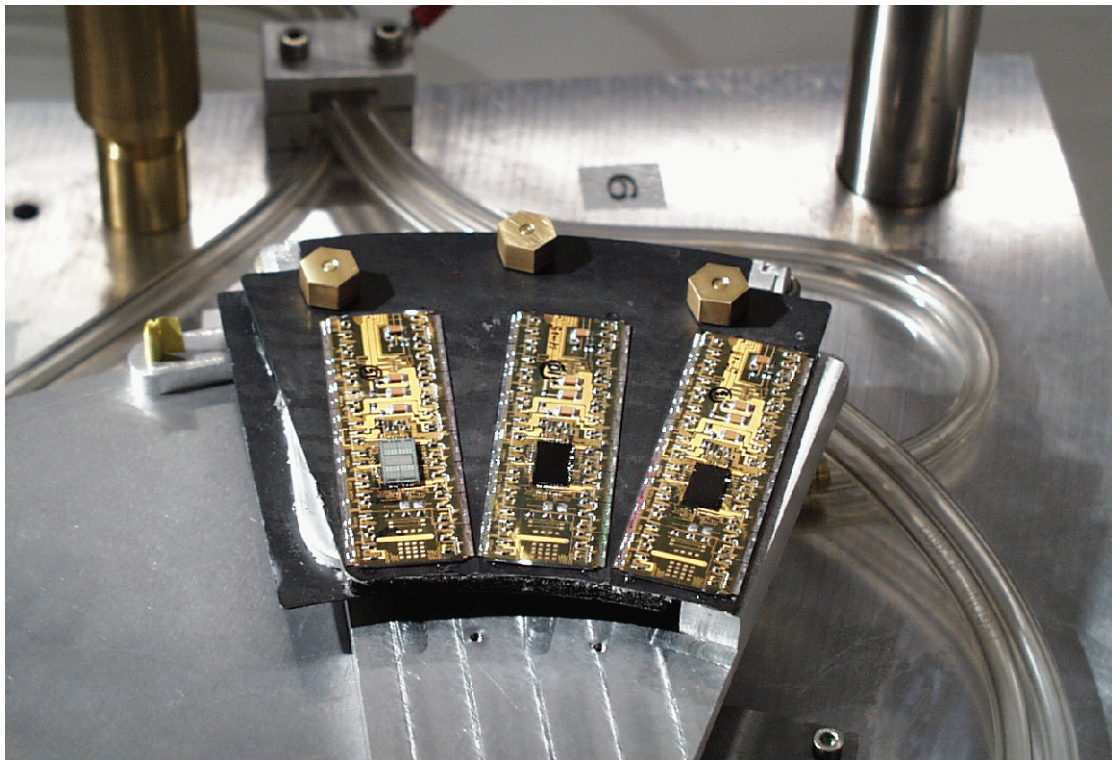
- Build up a complete half-sector to explore electrical integration issues.
- So far, one module has been completed and assembled onto a real disk sector prototype. It has been characterized in detail:



- Working on assembly of next two modules. We are comparing different Flex vendors, and different bump-bonding vendors. This work will be completed over the next few months, but will be repeated with new 0.25μ electronics.

Dummy modules:

- Collaborate in extensive “dummy module” program. US has supplied 200mm “dummy chip” wafers. Germany supplies “dummy sensors”. Daisy chain patterns are metalized onto wafers to allow testing bumping connectivity.
- A total of 100 modules, 50 with each bumping vendor, will be built to validate vendor production capability.
- These prototypes will be mechanically completely realistic, and will allow exercising production tooling and assembly concepts, plus making extensive tests of mechanical and thermal issues for complete modules.



Computing and Offline Software

Overall Architecture:

- Architecture Task Force created in ATLAS in 99, following overall Computing Review. Significant LBL participation (Quarrie and Shapiro), established direction for ATLAS, and recommended setting up Architecture team.
- Architecture team has five members, three from LBL, including Quarrie as Chief Architect.
- Two parallel goals: develop overall software Framework, and develop a full set of use cases to define requirements. Initial goal was Fall 2000 for functional prototype.

ATLAS Framework (ATHENA):

- New object-oriented framwork, to be used for all off-line activities, including simulation, reconstruction, and physics analysis.
- Also to be used in Event Filter (formerly known as Level 3 Trigger)
- Critical path for all software activities, with aggressive initial schedule.
- Decided to adopt LHC-B GAUDI framework as starting point. This has now led to productive collaboration between these two experiments on software.

Initial Framework prototypes and milestones:

May 2000 was first generation and included:

- Ability to read Physics TDR data (LBL)
- Ability to execute sequence of user modules, including dynamic loading of modules, and sequences with branches and filters (LBL).
- Prototype Event Generator framework (LBL)
- LArg reconstruction and XKalman tracking reconstruction (BNL + LBL)
- First support for fast simulation packages (London groups)

Feedack included:

- Series of three Event Data Model workshops in May, July, and October 2000
- Detector Description workshop in August 2000
- Tutorials: two at CERN and two at LBL, one at Frascati
- Architecture Review Committee (ARC), met in July, August, September, December 2000, and March 2001. Will deliver their report soon.

Sept 2000 was set for second set of milestones:

- Include use case analysis (LBL)
- Include ATHENA in ATLAS release machinery (LBL)
- Event Data Model prototype (LBL+BNL)
- Interactive Scripting prototype (LBL)
- Physics Analysis output to ROOT (LBL)
- Event Generators deployed (LBL)
- Objectivity I/O prototype (ANL+Orsay)

Dec 2000 was third set of milestones:

- Pileup prototype (LBL)
- Particle Properties service (FNAL + LBL)
- Physics Output to ROOT deployed (LBL)
- Objectivity I/O partially deployed (ANL+Orsay)
- Event Data Model, Interactive Scripting, and Fast Simulation deployed

Deliverable milestone dates basically all met

- Now a large and active developer community.
- C. Tull at CERN for one year, M. Marino to be at CERN for two years. Intend to have one person at all times to provide support.

Basic Functionality:

- Data is read from Permanent Store into Transient Store. System is independent from choice of database (Objectivity, ...)
- Data Objects are accessed from Transient Store
- Algorithms are controlled by framework and act on data. Examples could be Event Simulation, Pattern Recognition, or Higgs Analysis. Written by users, and initialized and executed by framework.
- Services are globally available components to be used by all algorithms (e.g. Histogramming, Random Numbers, Visualization, ...)

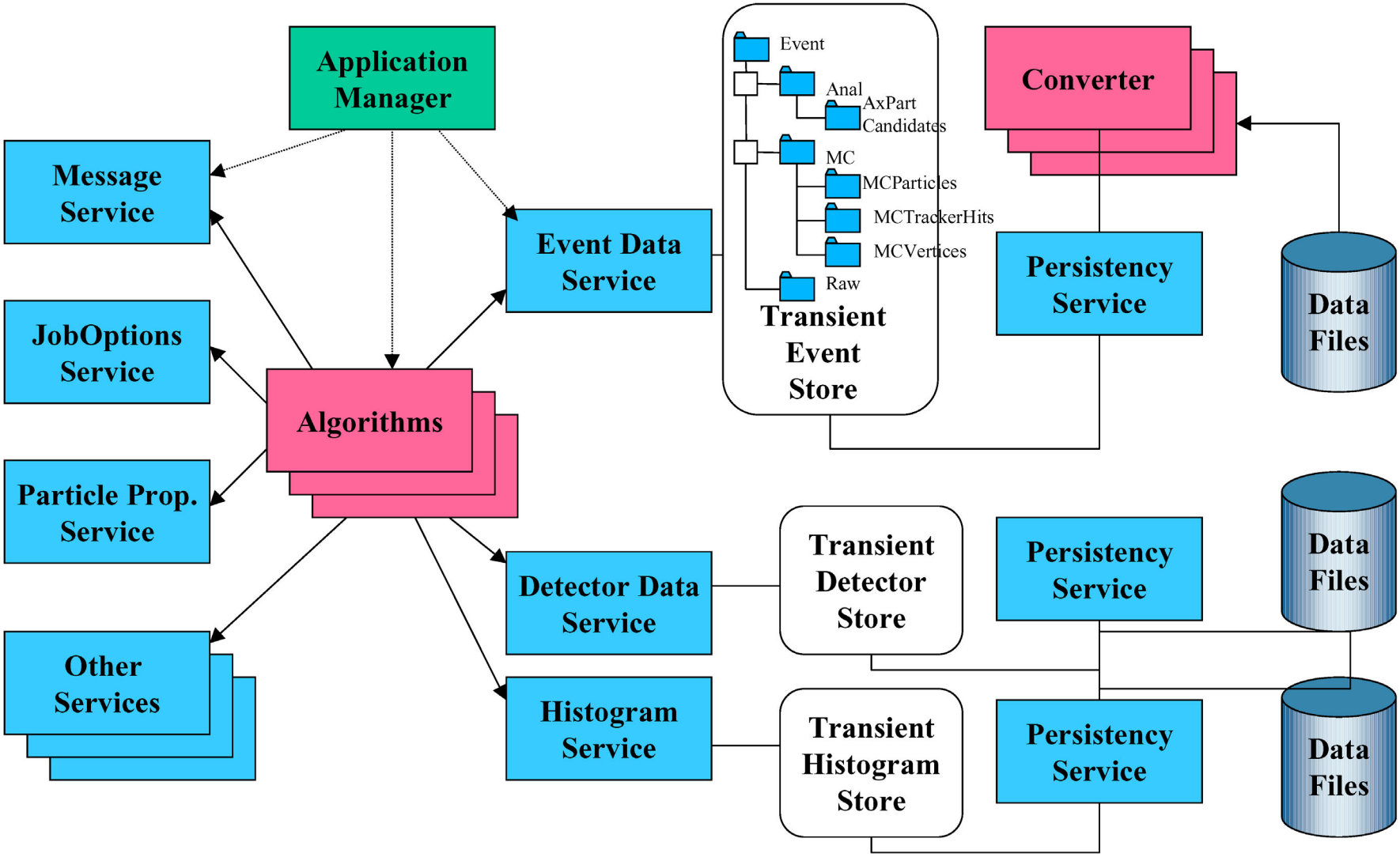
Next milestones:

- Use of ATHENA to prepare results for ATLAS Physics workshop in Sept 2001.
- Geant4 Integration prototype
- Visualization prototype
- Monitoring and Book-keeping prototypes

Prepare for Mock Data Challenge 1 (5% data sample):

- Production to start in Spring 2002.
- All prototypes discussed above should be fully deployed
- Mock Data Challenge 2 will follow late in 2002.

Structure of GAUDI/ATHENA:



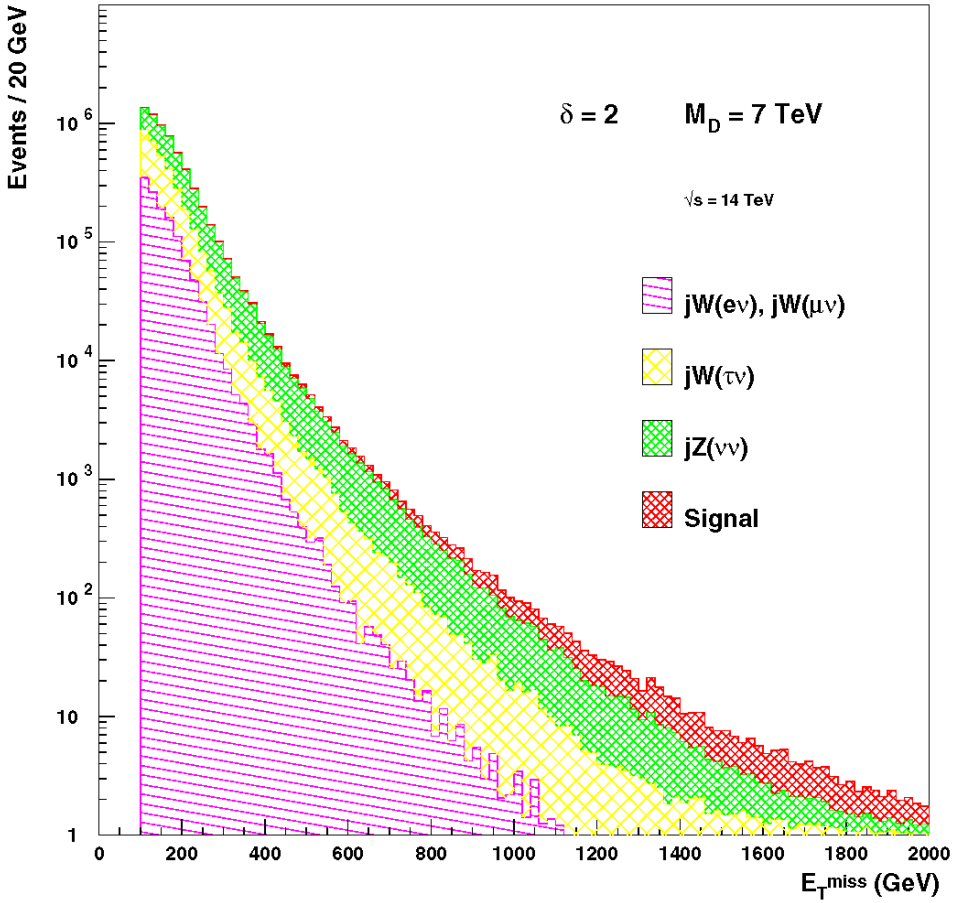
Physics Activities

Event/Physics Generators:

- LBL leads ATLAS Monte Carlo group, and is coordinating the installation of event generators, and their interfacing to ATHENA using HEPMC interface standard.
- Interface supports use of one generator for high PT event and a second for MinBias.
- Generators supported so far (by various individuals in ATLAS) include: PYTHIA, ISAJET, HERWIG, TAUOLA, VECBOS, and GENZ (old ATLAS format).
- Interface to ATHENA includes support for ATLAS-specific tunings, and the ability to pass and modify parameters at run-time.
- Significant effort required for support and integration of physics tools in ATHENA. Additional LBL manpower needed soon, or responsibilities will need to be dropped.

Search for extra dimensions:

- Many theories (e.g. strings) predict extra dimensions of size R (Arkani-Hamed...)
- A larger value of R allows the mass scale for gravity to be smaller, and still get the right strength. Models lead to “towers” of Graviton excitations.
- In simplest models, these G can be produced in association with a gluon or photon, leading to missing energy signatures.



Indication of the reach in mass (M_D) and number of extra dimensions (δ).

Signal starts to emerge above SM backgrounds at very large ET(miss).

This range of sensitivity corresponds to R as large as 10μ

Other physics studies, concentrating on SUSY issues:

- Significant work done for Physics TDR, indicating possibilities for doing precision SUSY physics with ATLAS.
- Ongoing studies on SUSY models with heavy squarks and sleptons (> 1.5 TeV, suppressing flavor changing currents), in which LHC would only be sensitive to "lighter" gluino and other gauginos. Particularly hard case to untangle models.
- Many SUSY models produce lots of tau's in their decay chains. The tau helicity then carries important information about sparticle masses and mixings. Full simulation study is ongoing to quantify to what extent this is really measurable.

Studies of LHC Upgrades:

- Request from CERN management to study LHC upgrades as part of long-range CERN plan. Hinchliffe is the only US participant for ATLAS.
- Directions include increase of E to 28 TeV and increase of L to 10^{35} $cm^{-2}s^{-1}$
- Pileup limits some physics at very high L, even for ideal detector. Examples include jet tagging in forward region, and ET(miss) resolution.
- Studies just beginning, but appears to be little additional physics reach for high L scenario unless detector performance can be maintained close to that at 10^{34}.

Issues for successful LBL ATLAS effort

- Role of labs like LBL in the US LHC effort is critical. US ATLAS relies heavily on the three “non-accelerator” labs (ANL, BNL, LBL) for its contributions. International HEP collaboration requires that they remain healthy.
- Pixel activity is a partnership with base program, capitalizing on extraordinary LBL teams in mechanics and electronics. Without a healthy base, this effort (and consequently ATLAS pixels) will fail.
- Computing effort is very strong, based on internationally unique LBL resources. US ATLAS computing is underfunded, and our strong base support of pixels prevents us from making any significant base committment to this effort. This core software is critical for ATLAS, and improved future support is needed.
- Physics simulation effort is strong, and also needs base resources to achieve a critical mass, and help pave the way for eventual major LBL role in LHC physics. Due to other constraints above, this is not happening.
- As of early June, LBL ATLAS group will have 2.5 postdocs (0.5 is in transition to CDF), and one UCB grad student (thesis will be on CDF). Starting in FY03, we must begin significantly ramping up this younger component of our effort to create a viable LBL ATLAS research program.

Continued erosion of LBL base support threatens our entire ATLAS effort.